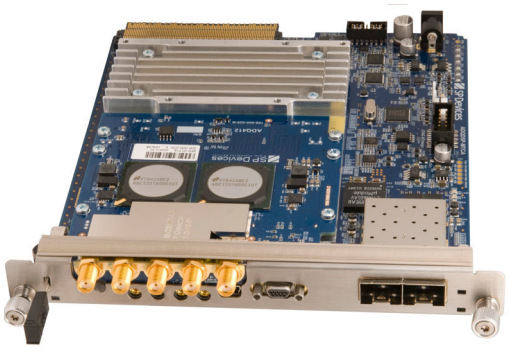
ADQ412

ADQ412 is a software-selectable 2 or 4 channel flexible member of the ADQ V6 Digitizer family. The ADQ412 has an outstanding combination of high bandwidth and dynamic range, which enables demanding measurements such as RF/IF sampling of very wide band signals. High bandwidth and high sample rate enable capture accurate of fast pulses.



Introduction

The ADQ412 is a flexible member in the ADQ V6 Digitizer family. It can be configured either as 2 or 4 analog input channels through a software control. There are several sample rate options; 2, 3.6 or 4 GSPS in 2-channel mode and 1, 1.8 or 2 GSPS in 4-channel mode. The vertical resolution is 12 bits. The analog input bandwidth is up to 2 GHz and a total of 700 Msamples data memory. The ADQ412 is optimized for dynamic performance over a wide bandwidth, which makes it ideal for broadband applications such as IF/RF sampling and high-speed data recording. The ADQ412 offers an easy-to-use API that allows easy integration into any application. The ADQ412 digitizer is available in several form factors to meet different systems integrations requirements; high-speed USB 2.0, cPCIe / PXIe, PCIe and Micro-TCA. The ADQ412 is equipped with an powerful Xilinx V6 LX240T FPGA which is partly available for customized real time applications.

ADQ412 Development Kit

SP Devices' ADQ412 Development Kit is an optional FPGA programming tool that rapidly enhance the customization process of your next DSP application for the onboard FPGA.

ADQ412 Development Kit enables real time signal processing of streaming data. More details about this product can be found in the product brief for the ADQ412 Development Kit.

Features

- Up to 4 analog channels
- Up to 4 GSPS sampling rate
- 12 bits resolution
- Up to 2 GHz analog bandwidth
- Internal and external clock reference
- Clock reference output
- External trigger input and output
- Multi record >1 MHz PRF
- Time stamp
- 700 Msamples data memory
- Data interface
  USB 2.0 / cPCIe / PXIe / PCIe / MTCA
- FPGA open for custom applications

Applications

- RADAR
- LIDAR
- Wireless communication
- Optical transmission
- High-speed data recording
- Test and measurement
- Ultrasonic ranging

Ordering information

ORDERING INFORMATION	
ADQ412	ADQ412
AVAILABLE OPTIONS	
Micro-TCA interface	–MTCA
cPCIe / PXIe interface	–PXIE
PCIe interface	–PCIe
High sampling rate	–3G
High sampling rate	–4G
RELATED PRODUCTS	
ADQ412 Development Kit	ADQ412 Dev Kit

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www.spdevices.com

1 Technical data[1]

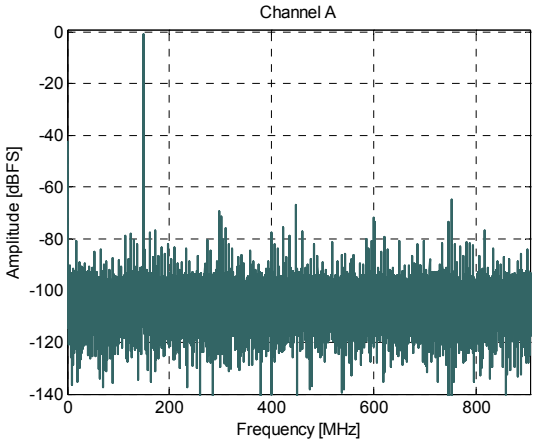
KEY PARAMETERS OVERVIEW	
Digitizer Resolution	12
Data memory	1 GByte
Trigger	Software / External / Level / Internal
Number of GPIOs	5
Front panel connectors	SMA/Micro-D Plug9w/MMCX
Clock source	Internal / External
Clock reference	Internal / External / PXIe

SAMPLE RATE OPTIONS OPTION	STD.	–3G	–4G	
4 CHANNELS MODE				
Number of channels	4	4	4	
Sampling rate	1	1.8	2	GSPS
Analog bandwidth	2	2	2	GHz
SFDR @149MHz	63	63	63	dBc
SNR @149MHz	57	57	55	dB
2 CHANNELS MODE				
Number of channels	2	2	2	
Sampling rate	2	3.6	4	GSPS
Analog bandwidth	1.3	1.3	1.3	GHz
SFDR @149MHz	60	60	63	dBc
SNR @149MHz	55	55	55	dB

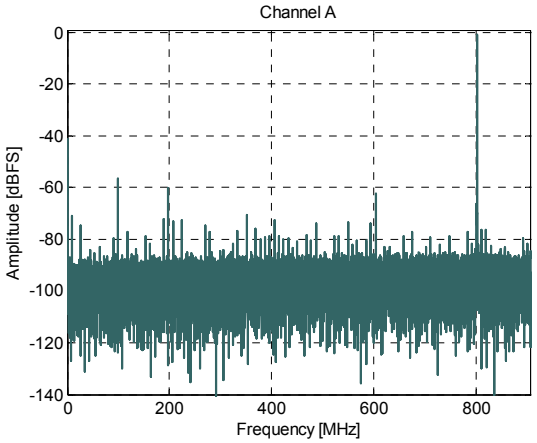
ANALOG INPUT		
Impedance AC	50	Ω
Input voltage range	800	mV_{pp}

2 Dynamic performance

2.1 Noise and distortion



SFDR	63	dB
SNR	57	dB
ENOB	8.7	bits

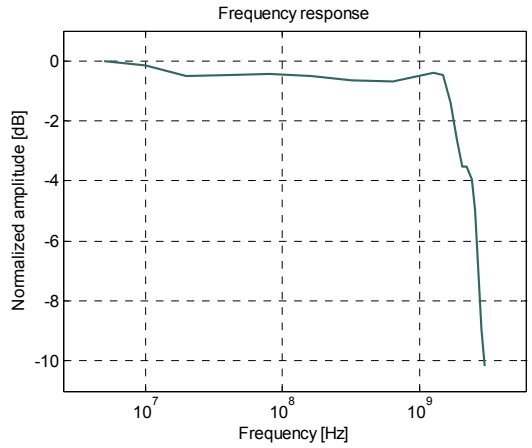


SFDR	55	dB
SNR	51	dB
ENOB	7.8	bits

Figure 1: FFT of 149 MHz and 801 MHz input signal at 1.8 GSPS.

1. All values are typical unless otherwise noted.

2.2 Frequency response



Bandwidth (–3 dB)	2 GHz
1 dB flatness	1.6 GHz

Figure 2: Frequency response in 4 channel mode.

3 Functional overview

3.1 Block diagram

The digitizer includes an analog front-end board with ADCs and a digital back-end board based on a Virtex 6 FPGA. This mezzanine structure allows for a large set of options on sample rate and form factor. The back-end controls the data flow, triggering and host communication.

3.2 Analog front-end

The ADQ412 can operate in a 4-channel mode where each ADC is connected to one analog input channel.

In the 2-channel mode, two ADCs operate on the same analog input in an interleaved mode. This doubles the sampling rate. The interleaving is enabled by ADX, see **Section 3.3**.

Since the capacitive load on the input is lower for the 4-channel mode, the input bandwidth is higher. This mode is suitable for RF/IF sampling in the first and second Nyquist band.

The 2 channel mode offers the largest digital bandwidth, and is suitable for sampling of high bandwidth modulated signals at a low IF. The high sample rate is optimized for capturing fast events, for example pulses.

The mode of operation is user controlled via software.

3.3 Interleaving ADX

The high data rate in 2-channel mode is enabled by SP Devices' technology for interleaving ADCs: ADX.

3.4 Digital back-end

Digital back-end is described in **Section 6**.

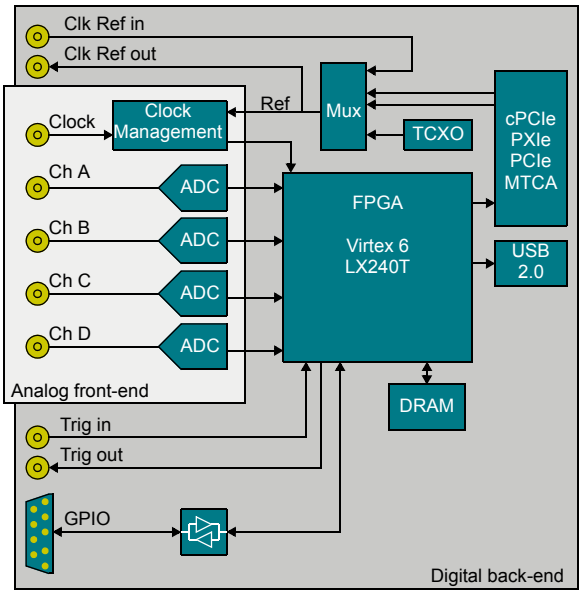


Figure 3: Block diagram 4 channel mode.

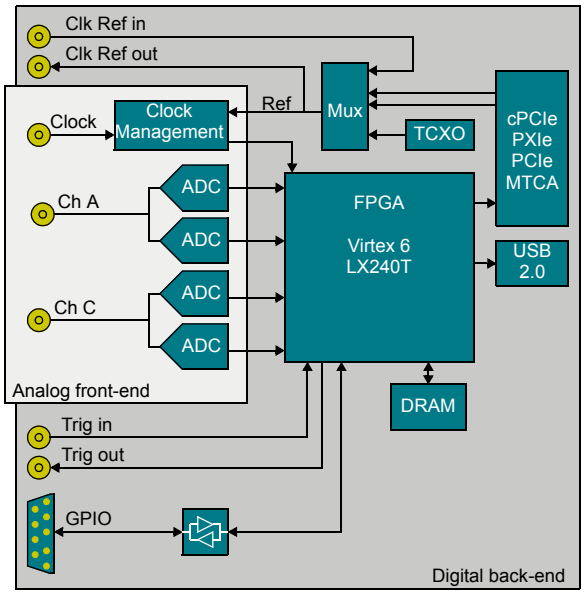


Figure 4: Block diagram 2 channel mode.

4 Absolute maximum ratings

Exposure to conditions exceeding these ratings may reduce lifetime or permanently damage the device.

The ADQ412 has a built-in fan to cool the device. If the air flow is blocked or the fan malfunctions, the temperature surveillance unit will protect the ADQ412 from overheating by shutting down parts of the device.

ABSOLUTE MAXIMUM RATINGS		
	Min	Max
Supply voltage (to GND)	–0.4 V	14 V
Trigger input (to GND)	–3 V	3.7 V
Clock ref (AC)		3.3 V_{PP}
Ambient temperature (operation)	0 ^{o}C	45 ^{o}C
Analog input (AC >1KHz)		5 V_{pp}
Analog input DC	–2.5 V	2.5 V

5 Sample rate options

The ADQ412 is available with several sample rates options. The option determines the maximum sample rate. See **Section 1** for technical data.

The order code for 3.6 GSPS option is

Order code: –3G

The order code for 4 GSPS option is

Order code: –4G

6 Digital back-end

6.1 Architecture

The control and processing part of the digitizer is done in a Xilinx Virtex 6 LX240T FPGA. Parts of the FPGA are available for customized real-time applications through the ADQ412 Development Kit.

The digital back-end controls triggers, clock reference sources, GPIO, data storage and host interface. See **Section 6.2** for a technical specification.

There is 1 GByte data memory. For more information about memory handling, see **Section 9.6**.

There are several clock reference sources, and the board has connectors for external clock reference input and output. See **Section 8** for details about the clock system.

The triggering is handled by the digital back-end. The board has connectors for external trigger input and output. See **Section 9** for details about the trigger system.

The GPIO connector is described in **Section 7**.

There are several host interface options available. The photo in **Figure 5** is an example of a cPCIe/PXIe interface. See **Section 11** for details about the host interfaces.

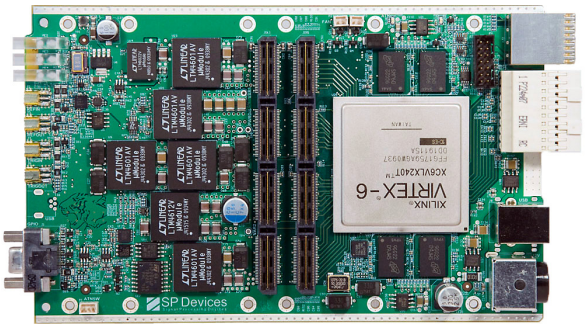


Figure 5: Photo of Digital backend (PXIe format)

6.2 Technical data[1]

INTERNAL CLOCK REFERENCE	
Clock reference sources	10 MHz external
	Internal TCXO

EXTERNAL CLOCK REFERENCE		
Frequency (min – max)	10	MHz
Signal level (min – max)	0.8 – 3.3	V_{PP}
Impedance AC	50	Ω
Duty cycle	50% ± 5%	
Connector	MMCX	

CLOCK REFERENCE OUTPUT		
Frequency (min – max)	10	MHz
Signal level	3.3	V_{PP}
Impedance AC	50	Ω
Duty cycle	50% ± 5%	
Connector	MMCX	

POWER SUPPLY		
Supply voltage	12	V
Power consumption	36	W

MEMORY	
Data memory	1 GByte
Pre-trigger buffer	Up to batch size
Trigger hold-off	2^{34} samples
Multi record batch size	Up to memory size
Multi record max PRF	>1 MHz

EXTERNAL TRIGGER INPUT		
Input impedance DC	50	Ω
Input range (min – max)	–2.5 – +3.3	V
Threshold rising/falling edge	0.5	V
Time resolution	250	ps
Connector	MMCX	

TRIGGER OUTPUT		
Output impedance	30	Ω
Output (low – high)	0.1 – 3.2	V
Connector	MMCX	

1. All values are typical unless otherwise noted.

GPIO		
Number of GPIO	5	
Output impedance	30	Ω
Output (low – high)	0.1 – 3.2	V
Input impedance	10	kΩ
Input (low – high)	1 – 2.3	V
Connector	Micro DSUB 9 way	

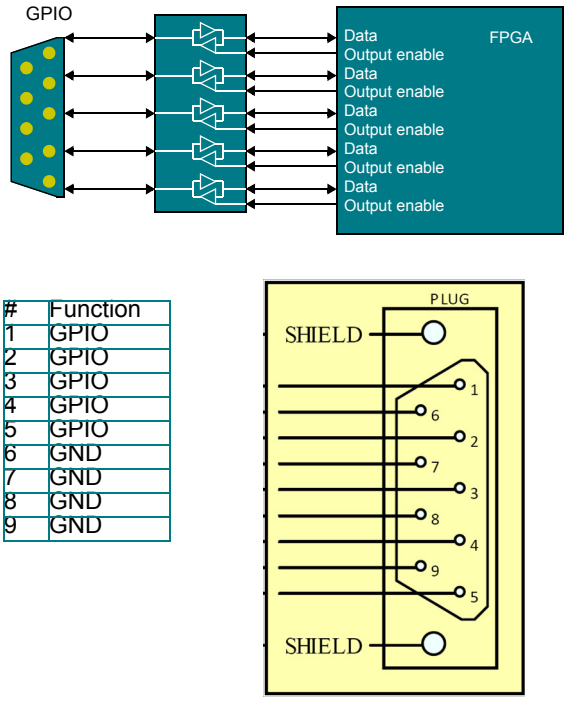
ENVIRONMENTAL / MECHANICAL		
Operating temperature	0 – 45	°C
Storage temperature	–20 – 70	°C
Relative humidity, non-condensing	5% – 95%	

CERTIFICATION AND COMPLIANCE
CE

7 GPIO

The ADQ412 is equipped with 5 bidirectional GPIOs. The GPIOs are controlled from software, but can also be accessed from the ADQ412 Development Kit.

The connector is Micro DSUB plug 9 way. A suitable socket with lead is for example MOLEX 83421-9044.



#	Function
1	GPIO
2	GPIO
3	GPIO
4	GPIO
5	GPIO
6	GND
7	GND
8	GND
9	GND

Figure 6: GPIO block diagram.

8 Clock

8.1 Clock system

A typical ADQ V6 Digitizer family clock implementation is shown in **Figure 7**. The clock system consist of reference part and a generation part.

The selection of clock reference source is placed on the motherboard to support different daughter boards. Various combinations of sources are available based upon selection of the digital interface to the host.

The reference is sent to the PLL on the daughter board. The PLL is placed on the daughter board to support the specific ADC and its range of selectable sample rates. The data clock out from the ADC is sent to the MRCC pin of the FPGA, and used as a system clock in order to keep the digitizer synchronous to the data rate.

There is also a direct external clock input to the digitizer, for which the PLL is used only for distribution of the clock.

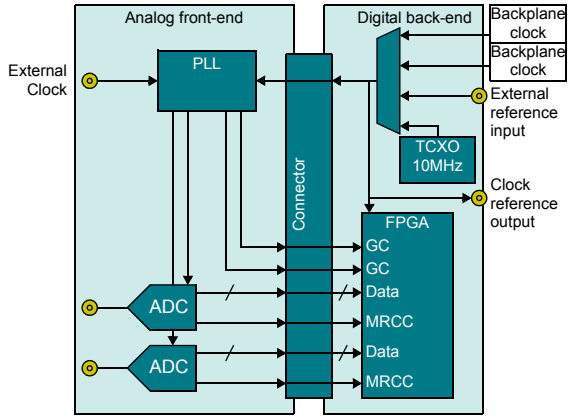


Figure 7: Clock of daughter board. Typical digitizer solution.

8.2 Clock reference sources

The available references for different host interfaces are listed in the table.

SOURCES	USB	PXIE	PCIE	MTCA
10 MHz TCXO	Yes	Yes	Yes	Yes
External	Yes	Yes	Yes	Yes
PXIe 100MHz		Yes		
Micro-TCA backplane				Yes, 2

The internal clock reference (TCXO) is for stand alone operation.

The external clock reference and backplane clocks are used for implementing phase locked systems.

8.3 External clock input

There is a clock input for direct external clocking of the digitizer. The PLL on the ADQ412 is only used for distributing the clock. The clock frequency is set differently for the 2-channel and 4-channel modes, see below.

EXTERNAL CLOCK FREQUENCY	
4-channel mode	Sampling clock frequency
2-channel mode	Sampling clock frequency / 2

8.4 Clock reference output

The selected clock reference is available through a front panel connector for driving other external equipment.

8.5 Synchronizing units

Several ADQ412 units may be synchronized. Using the external inputs for a common clock reference or common direct clock will maintain phase stability between units.

A common external trigger input synchronizes the units to start simultaneously.

9 Trigger and Acquisition

9.1 Overview

The digitizer can operate in a batch wise acquisition mode, where the data capture is controlled by a trigger event. One data record of limited length is recorded at each trigger and the sequence of operation is the following:

1. Arm
2. Wait for trigger
3. Trigger
4. Acquire data
5. Re-arm / stop

When armed, the system is waiting for the selected trigger event. At the trigger event, a data record of selected length is recorded in the data memory. After the acquisition, the digitizer is either re-armed (see **Section 9.6**) or stopped.

There are several options for trigger event

- Software trigger
- Level trigger
- External trigger
- Backplane trigger
- Daughter board dedicated trigger

The size and timing of the data record is user-controlled through the parameters

- record length
- number of records
- trigger hold-off
- pre-trigger buffer length

The record length defines the total amount of data at each trigger. The trigger hold-off and the pre-trigger positions the data record relative the trigger event. The pre-trigger buffer is a part of the total record length and is thus limited to the record length, whereas trigger hold-off is not depending on the record length. One acquisition can contain several records, that is the multi-record mode, see **Section 9.6**.

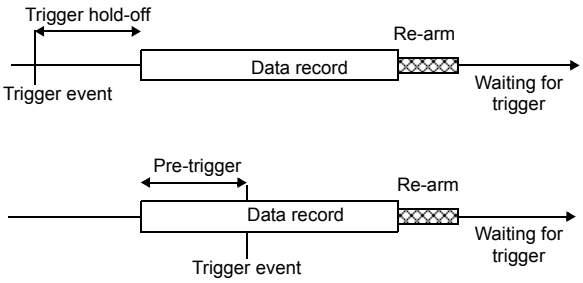


Figure 8: Trigger timing

9.2 Functional properties

TRIGGER PARAMETERS		
External trigger time resolution	1	samples
Max record length	Up to memory size	
Pre–trigger	Up to record size	
Trigger hold-off	2^{31}	Samples
Re-arm time	300	ns
Record header	64	bytes

9.3 Trigger sources

9.3.1 External trigger input

Data capture is triggered by positive or negative edge on the trigger input connector. The external trigger is intended for synchronous systems[1], where the signal source is phase locked to the ADQ412. It can also be used for synchronizing several ADQ412 digitizers. The trigger time resolution is depending on the sample clock.

The trigger input is DC coupled with 50 Ohm termination. The trigger threshold is fixed at 0.5 V for both rising and falling edge detection. The connector type is MMCX.

9.3.2 Software trigger

Data capture is triggered by a software command. This is suitable for measurements on continuous waves.

9.3.3 Level trigger

Data capture is triggered by an event on the input data This is useful for capturing pulses. A trigger

1. In a synchronous system, the trigger jitter parameter is not relevant. The cable length will influence jitter timing.

is generated when the data values passes a user defined level. The level trigger can operate on rising and falling edges. A user-controlled noise suppression function removes false triggers. The level trigger combined with the pre-trigger or trigger hold-off setting can capture any pulse shape.

9.3.4 Internal trigger

The internal trigger is a synchronous trigger signal with a programmable repetition rate. The internal trigger may both trigger the digitizer as well as external equipment through the trigger output.

9.4 Trigger output

The trigger output is a high current short-circuit protected digital output signal which makes the trigger available for external equipment. The trigger output can be used for broadcasting triggers to several ADQ412 boards which increase the channel count in the measurement system. It may also be used for triggering a signal source in the measurement setup.

9.5 Time stamp

A 64-bit time counter, which runs at the sampling frequency, enables a time stamp for each event. At each trigger event, the counter value is read and stored together with the data record.

The time counter starts at power up and may directly be used for relative time measurement. At any time, the counter may be reset by software. The counter can also be synchronized to an external start pulse. The external start pulse can operate in two modes; single start signal or repeated restart of the time counter.

A single start mode is intended for aligning the time counter in several units.

The repeated restart mode is intended for synchronizing the time counter with external equipment, for example a GPS 1PPS signal. The counter is then divided into a 42 bits time counter and a 22 bits start pulse counter. At each start pulse, the time counter is restarted from zero and the pulse counter is increased by one. The reset/start pulse is connected to GPIO pin #2 through a setup register.

9.6 Multi-record mode

The ADQ412 can be set up in a multi-record mode. At each trigger, a record of data is captured in the memory. The length of each record and number of records is user defined. Multi-record can be used together with pre-trigger buffer and trigger hold-off.

To each record belongs a 64-byte header with trigger information and time stamp data.

9.7 Streaming data to disk

The ADQ412 can stream data directly to HDD. The data rate from the ADCs is, however, to high to be streamed directly to a HDD. There are several ways of reducing the data rate. The pre-installed data reduction is batch wise acquisition, where a limited amount of data is buffered on each trigger[1].

Custom data reduction, such as filtering, peak detection etc., may be implemented using the ADQ412 Development Kit.

1. The difference to multi-record mode is that the data memory on the digitizer is by-passed, which result in a higher throughput.

10 Software tools

10.1 Operating systems

The software includes drivers for several platforms. The Linux support is limited[1].

OPERATING SYSTEM	
Windows XP	SP 2 and higher
Windows Vista	All versions
Windows 7	32 bit and 64 bit
Linux	Limited support

APPLICATION SOFTWARE	
ADCaptureLab	Data capture and analysis
MATLAB	Data capture API
C/C++	Data capture API

10.2 ADCaptureLab

The ADQ412 is supplied with the ADCaptureLab software that provides quick and easy control of the digitizer. The tool also offers both time domain and frequency domain analysis, see **Figure 9**. Data can be saved in different file formats for off-line analysis. Comparison of results is easily done by importing data from file and analyzing it in ADCaptureLab. With ADCaptureLab, the ADQ412 operate as a desktop oscilloscope.

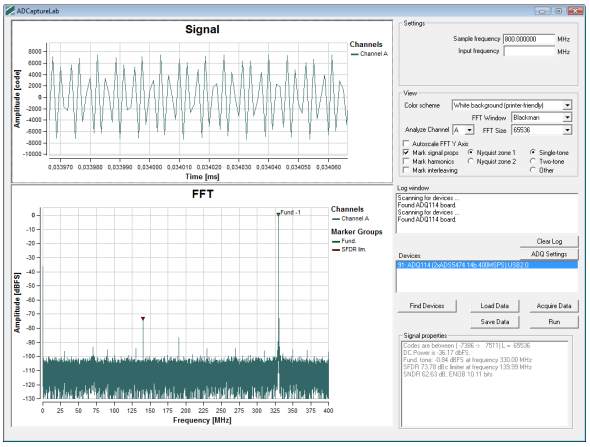


Figure 9: ADCaptureLab (Typical)

10.3 Software development kit (SDK)

The ADQ412 digitizer is easily integrated into your own application by using the software development kit. The SDK is included with the ADQ412.

The SDK includes programming examples and reference projects for C/C++ and MATLAB. The ADQAPI users guide in detail describes all functions. Many examples and application notes simplify the integration process.

Using the SDK enables rapid custom processing of large amounts of data and real-time control of the digitizer.

1. Contact an SP Devices sales representative for information on supported releases.

11 Digital interface options

The ADQ V6 digitizer family supports various number of interfaces. The digital interface is used for control and data transfer between the host and the digitizer.

11.1 Firmware upgrade interface

Regardless of the selected data interface, there is always an additional USB interface for firmware upgrade. This connection is not related to the data and control interface

11.2 USB interface

With the USB interface, the digitizer is easily connected to any computer.

USB INTERFACE		
Standard	USB 2.0	
Data rate sustained	25	MB/s
Box size	53 x 106 x 166	mm3

(a) Front panel

(b) Rear panel

Figure 10: Typical USB interface unit

11.3 cPCIe / PXIe interface

The ADQ412 is available with cPCIe / PXIe interface.

cPCIe / PXIe INTERFACE		
Bus width	8	lanes
Bus peak capacity	16	Gbit/s
Sustained data rate	400	MByte/s
PXIe card size	3U 2 slot 8TE	

Figure 11: cPCIe / PXIe card

Order code: –PXIE

11.4 PCIe interface

The ADQ412 is available with PCIe interface.

PCIe INTERFACE		
Bus width electrical	8	lanes
Bus peak capacity	16	Gbit/s
Sustained data rate, 8 lanes	TBD	MByte/s
Bus width mechanical[1]	16	lanes
Board height	2	slots

1. The wide contact is required to support the weight of the board.

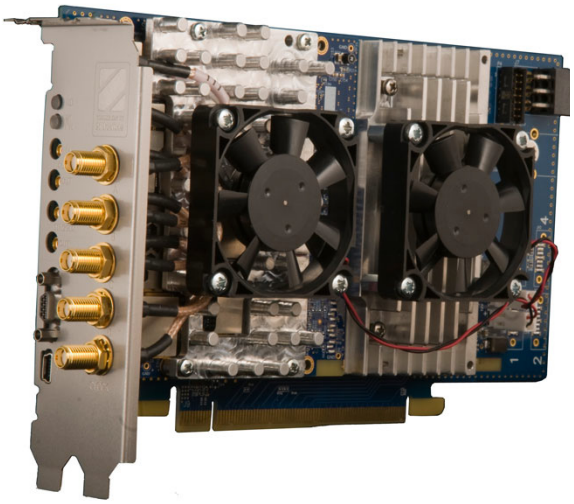


Figure 12: PCIe card.

Order code: –PCIe

11.5 Micro-TCA interface

The ADQ V6 Digitizer family is available with digital back-end and interfaces for Micro-TCA.

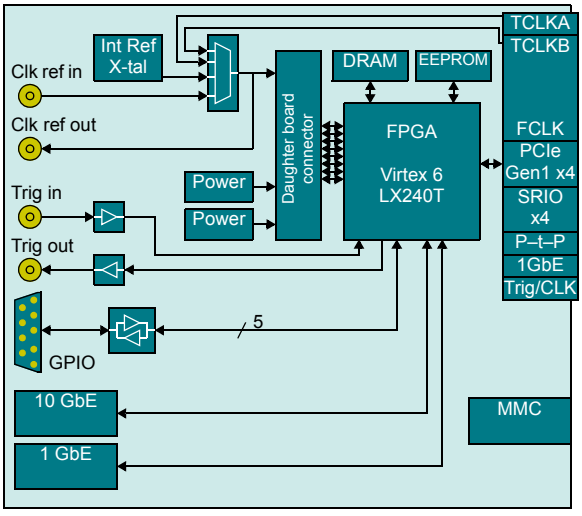


Figure 13: Block diagram of digital back-end for Micro-TCA.

MICRO-TCA BOARD SIZE	
Board width	Double width
Board height	Mid-size

Some of the pins in the backplane connector are used for the standard digitizer functions. Some are available for custom design using the ADQ412 Development Kit for custom implementations.

MICRO-TCA INTERFACE		
Signal	Port	Status
1GbE	0	ADQ412 Dev Kit
PCIe	4-7	Standard
Point-to-point	12-15	ADQ412 Dev Kit
Trigger, Data, Clocks	17-20	ADQ412 Dev Kit
TCLKA	Clk 1	Standard
TCLKB	Clk 2	Standard
FCLKA	Clk 3	Standard

FRONT PANEL ADDITIONAL INTERFACE		
Signal	Connector	Status
1 GbE	SFP	ADQ412 Dev Kit
10 GbE	SFP+	ADQ412 Dev Kit

Figure 14: Micro-TCA card.

Order code: –MTCA