PAUL SCHERRER INSTITUT

9 Channel, 5 GSPS Switched Capacitor Array

DRS4

FEATURES

Single 2.5 V power supply
Sampling speed 700 MSPS to 5 GSPS
8+1 channels with 1024 storage cells each
Cascading of channels or chips allows deeper sampling depth
Differential inputs with 950 MHz bandwidth
Differential outputs for direct ADC interfacing
Transparent mode for integrated triggering
Readout time: 30 ns * number of samples
Simultaneous reading and writing
Multiplexed or parallel analog outputs
Low power: 140 mW typical at 2 GSPS (17.5 mW per channel)
Low integral nonlinearity: 0.5×10^{-3} at 1 V range
High SNR: 69 dB after offset correction
Low Noise: 0.35 mV after offset correction

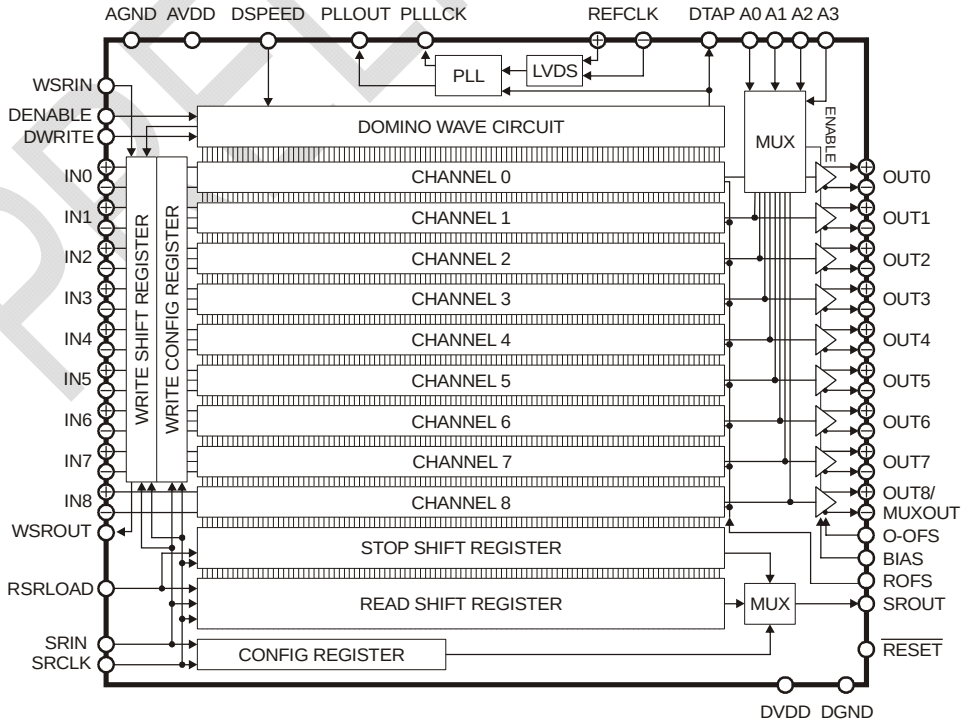
APPLICATIONS

Instrumentation and Measurement
Photomultiplier, Drift Chamber and APD Readout
Low Cost Digital Oscilloscopes
Ultrasound Equipment

GENERAL DESCRIPTION

The Domino Ring Sampler (DRS) is a switched capacitor array (SCA) capable of sampling 9 differential input channels at a sampling speed of 700 MSPS to 5 GSPS (6 GSPS for selected chips). The analog waveform is stored in 1024 sampling cells per channel, and can be read out after sampling via a shift register clocked at 33 MHz for external digitization.
The write signal for the sampling cells is generated by a chain of inverters (domino principle) generated on the chip and stabilized by a PLL. The domino wave is running continuously until stopped by a trigger. A read shift register clocks the contents of the sampling cells either to a multiplexed or to individual outputs, where it can be digitized with an external ADC. It is possible to read out only a part of the waveform to reduce the digitization time.
The high channel density, high analog bandwidth of 950 MHz, and low noise of 0.35 mV (after offset calibration) makes this chip ideally suited for low power, high speed, high precision waveform digitizing. Fabricated on an advanced CMOS process in a radiation hard design, the DRS4 is available in a 76-pin quad flat non-leaded package (QFN).

FUNCTIONAL BLOCK DIAGRAM



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REVISION HISTORY

04/1/2008-Revision 0: Initial Version
05/1/2008-Swapped out+ / out- pins
05/27/2008-Introduced QFN76 package
09/11/2008-Corrected MUXOUT location
09/15/2008-Added bandwidth and impedance
10/1/2008-Added power requirements
10/7/2008-Added S/H timing requirements
10/7/2008-Added Read Shift Register Initialization
10/13/2008-Added description of analog outputs
10/17/2008-Introduced Aperture Jitter
11/3/2008-Added BIAS, O-OFS impedance, differential gain
11/19/2008-Small exposed pad in package
11/28/2008-Corrected maximal sampling speed from 5 GSPS to 6 GSPS
12/23/08-Corrected maximal sampling speed from 6 GSPS back to 5 GSPS. Added few more parameters
2/11/09-Corrected wrong pin labels for P76 and P19, mention initialization of domino circuit
5/29/09-Updated all old plots
7/7/09-Added note about DENABLE/DWRITE pull-down resistors
7/9/09-Added range of ROFS signal

SPECIFICATIONS

(AVDD = 2.5 V, DVDD = 2.5 V, Temp. = 25°C, unless otherwise noted)

Table 1.

Parameter	Typ.	Unit	Comment
DRS4			
Sampling speed f_{SAMP}	0.7	GSPS min	
	5	GSPS max	Guaranteed
	6	GSPS max	Selected chips
Readout speed	10	MHz min	Optimal Performance at 33 MHz
	40	MHz max	At reduced linearity
	30 * (*n*+1)	ns	ROI readout mode for *n* cells
Fixed pattern offset error	5	mV rms	
Random noise	0.35	mV rms	After offset correction
Signal-to-Noise Ratio (SNR)	69.1	dB	After offset correction
Effective number of bits	11.5	Bits	After offset correction
Gain	0.982	V/V min	
	0.988	V/V max	
Integral Nonlinearity	0.5	mV	BIAS = 0.70 V, 33 MHz
	1.5	mV	BIAS = 0.70 V, 40 MHz
	22	mV	BIAS = 0.70 V, 50 MHz
Fixed pattern aperture jitter	TBD	ps	f_{SAMP} = 0.5 GHz
	TBD	ps	f_{SAMP} = 2 GHz
	TBD	ps	f_{SAMP} = 5 GHz
Random aperture jitter	TBD	ps	f_{SAMP} = 0.5 GHz
	TBD	ps	f_{SAMP} = 2 GHz
	TBD	ps	f_{SAMP} = 5 GHz
PLL jitter	25	ps	f_{SAMP} = 5 GHz
	285	ps	f_{SAMP} = 1 GHz
TEMPERATURE DRIFT			
Offset Error	75	µV/°C	Tested between 25° C and 50° C
Gain Error	25	ppm/°C	Tested between 25° C and 50° C
ANALOG INPUTS			
Differential Input Span	1	V p-p	
Common mode Range	0.1 – 1.5	V	
Absolute Voltage Limits	AGND – 300 mV	V min	
	AVDD + 300 mV	V max	
Input Capacitance	7	pF	Betw. IN+ and IN-, Domino Wave stopped
	11	pF	Betw. IN+ and IN-, Domino Wave running, value by design only[1]
	15	pF	Betw. IN+ and GND, Domino Wave stopped
Static Input Current	1.4	nA	Measured with DMM at 1V input
Dynamic Input Current	80	µA	f_{SAMP} = 0.5 GHz, U_{in}=1V
	320	µA	f_{SAMP} = 2 GHz, U_{in}=1V
	800	µA	f_{SAMP} = 5 GHz, U_{in}=1V
Equivalent input impedance	6.3	kΩ/f_{SAMP}[GHz]	
Bandwidth (-3dB)	950	MHz	
Crosstalk adjacent channels	< -46	dB	1 ns rise-time pulse driven differentially
	-40	dB	1 ns rise-time pulse driven non-differentially
DSPEED input impedance	> 10	GΩ	
BIAS input impedance	1	kΩ	Must be connected to a low impedance source to override the internal 0.7V
O-OFS input impedance	9	kΩ	Must be connected to a low impedance source to override the internal 1.37V
ROFS input impedance	> 50	MΩ	Static current. For proper dynamic operation, this input must be connected to a high speed low impedance source
ROFS Range	0.1 – 1.6	V	Limited by internal NMOS switch
ANALOG OUTPUTS			
Common mode voltage	1.37	V	Can be changed via O-OFS

[1] Due to the switching capacitors the input capacitance is non-constant and cannot be measured reliably. The value is derived from the capacitance with Domino Wave stopped and the fact that 16 input cells with 0.15 pF are on during sampling.

Bandwidth (-3 dB)	50	MHz	All measured in Transparent Mode
Offset Voltage	###	mV	
Offset Voltage Drift	###	μV/°C	
LOGIC LEVELS			
High Level Input Voltage	2.0	V min	
	2.8	V max	Chip is **not** 3.3 V tolerant
Low Level Input Voltage	0.8	V max	
High Level Input Current	±1.5	nA	
Low Level Input Current	±1.5	nA	
Input Capacitance	6	pF min	
	60	pF max	
High Level Output Voltage	2.47	V	IOH = 100 μA
High Level Output Voltage	2.26	V	IOH = 1 mA
Low Level Output Voltage	0.003	V	IOL = 100 μA
Low Level Output Voltage	0.08	V	IOL = 1 mA
TIMING CHARACTERISTICS			
$\mathbf{t_{DTAP}}$	$2048 \times 1/f_{SAMP}$	s	
$\mathbf{t_{CLK}}$	1	μs max	Clock speed for all shift registers
	2	ns min	
$\mathbf{t_O}$	10	ns	SRCLK Rising Edge to Analog Output
$\mathbf{t_{RESET}}$	10	ns min	Minimum width of negative reset pulse
$\mathbf{t_{SAMP}}$	t_O+t_{CLK}		For optimal performance, use t_{CLK}=30 ns and sample analog signal 38 ns after SRCLK
$\mathbf{t_{DSTOP}}$	10	ns min	DWRITE falling edge to DENABLE falling edge
$\mathbf{t_S}$	5	ns min	Setup time between A3-A0 and SRCLK
$\mathbf{t_H}$	5	ns min	Hold time between SRIN and SRCLK
POWER REQUIREMENTS			
AV_{DD}	2.5 ± 5%	V	
DV_{DD}	2.5 ± 5%	V	
DI_{DD}	<15	μA	A3-A0=1 (Standby mode)
	5.2	mA	Domino wave stopped
	38	mA	Running at 1 GSPS
	49	mA	Running at 2 GSPS
	92	mA	Running at 6 GSPS
	40	mA	Additional to the values above if transparent mode is on
AI_{DD}	<1	μA	A3-A0=1 (Standby)
	5.2	mA	Running at 1 GSPS
	6.1	mA	Running at 2 GSPS
	9.1	mA	Running at 6 GSPS
Power dissipation	110	mW	1 GSPS, transparent mode off
	350	mW	6 GSPS, transparent mode on

PIN FUNCTION DESCRIPTIONS

Table 2. Pin Function Descriptions

Pin Number	Mnemonic	Description
3,5,7,9,11,13,15,17,20	IN0+ – IN8+	Analog Input Channels 0 – 8 (+)
4,6,8,10,12,14,16,18,21	IN0- – IN8-	Analog Input Channels 0 – 8(-)
19,22,39,44,53	DGND	Digital Ground
23,24,33,34	DVDD	Digital Power Supply, 2.5 V Nominal
25	WSROUT	Double function: Write Shift Register Output if DWRITE=1, Read Shift Register Output if DWRITE=0.
26	SROUT	Multiplexed Shift Register Output
27	SRIN	Shared Shift Register Input
28	SRCLK	Multiplexed Shift Register Clock Input
29	RSRLOAD	Read Shift Register Load Input
30	ROFS	Read Offset Voltage Input. Used to shift the contents of the sampling capacitors into the linear range of the output buffers.
31,32,60,61	A0,A1,A2,A3	Address Bit Inputs, see *Table 1*
35	$\overline{\text{RESET}}$	Reset input. Leave open to utilize internal reset.
36	O-OFS	OUT- offset. Use internal voltage of nominal 1.25V if lept open. If connected to a low impedance voltage source overwrites the internal voltage.
40,43,45,48,49,52,54,57	OUTx+	Analog Output Channel 7 – 0 (+)
41,42,46,47,50,51,55,56	OUTx-	Analog Output Channel 7 – 0 (-)
37	MUX+/OUT8+	Multiplexed Analog Output/Analog Output Channel 8 (+)
38	MUX-/OUT8-	Multiplexed Analog Output/Analog Output Channel 8 (-)
1,2,58,64,70	AGND	Analog Ground
59,65,71,76	AVDD	Analog Power Supply, 2.5 V Nominal
62	DTAP	Domino Tap Signal Output toggling on each domino revolution
63	PLLLCK	PLL Lock Indicator Output
66	REFCLK+	Reference Clock Input LVDS (+)
67	REFCLK-	Reference Clock Input LVDS (-)
68	PLLOUT	PLL Output, to be fed to DSPEED via loop filter
69	DSPEED	Analog Voltage Input for Setting Domino Speed
72	BIAS	Bias voltage for internal buffers. Use internal voltage of nominal 0.7 V if left open. If connected to a low impedance voltage source overwrites the internal bias voltage.
73	DWRITE	Domino Write Input. Connects the Domino Wave Circuit to the Sampling Cells to enable sampling if high.
74	DENABLE	Domino Enable Input. A low-to-high transition starts the Domino Wave. Setting this input low stops the Domino Wave.
75	WSRIN	Write Shift Register Input. Connected to WSROUT of previous chip for chip daisy-chaining

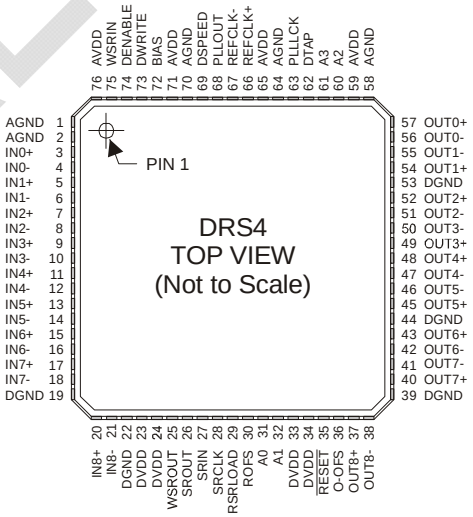
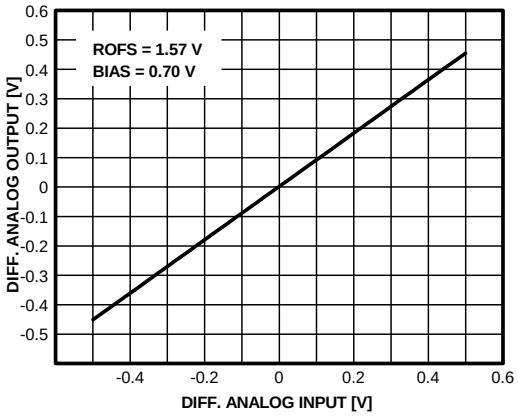
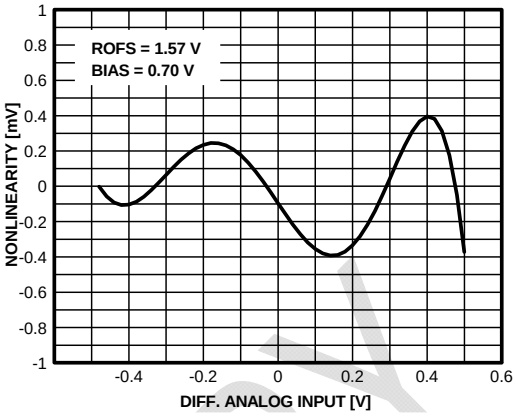


Figure 1. 76-Lead QFN Pin Configuration, Top View

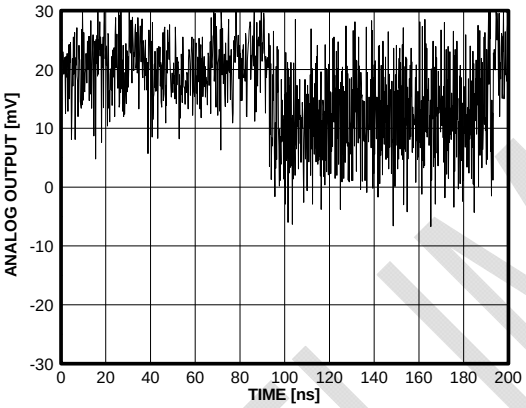
TYPICAL PERFORMANCE CHARACTERISTICS



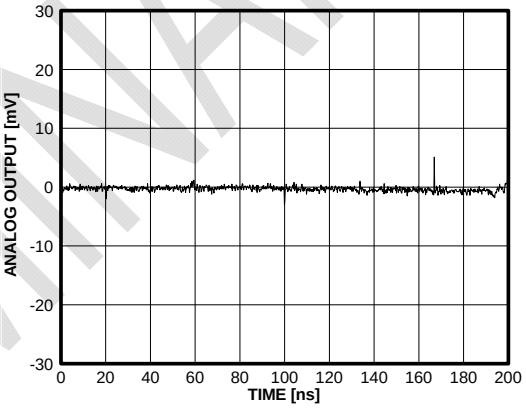
Plot 1. Analog Output vs. Analog Input



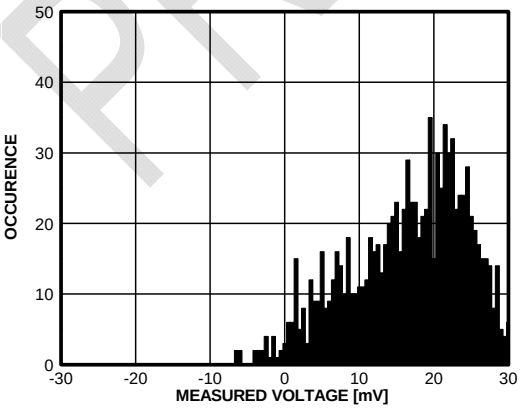
Plot 2. Typical Nonlinearity after Offset and Gain Calibration



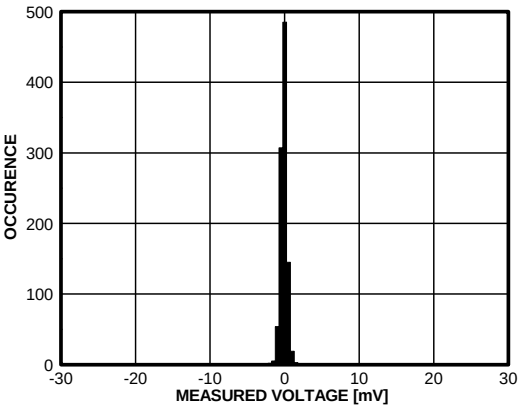
Plot 3. 0 V DC signal sampled at 5 GSPS before offset correction



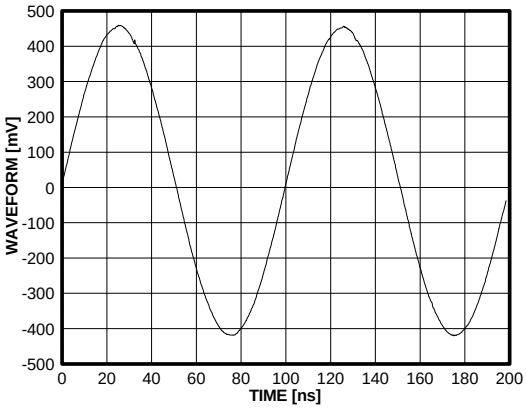
Plot 4. 0 V DC signal sampled at 5 GSPS after offset correction. The spike at ~170 ns originates from some crosstalk from the USB interface on the evaluation board



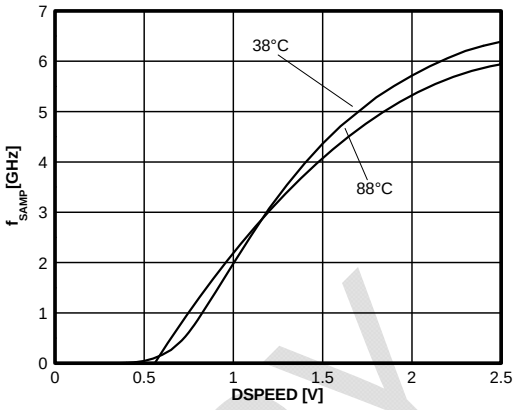
Plot 5. Noise Histogram before offset correction



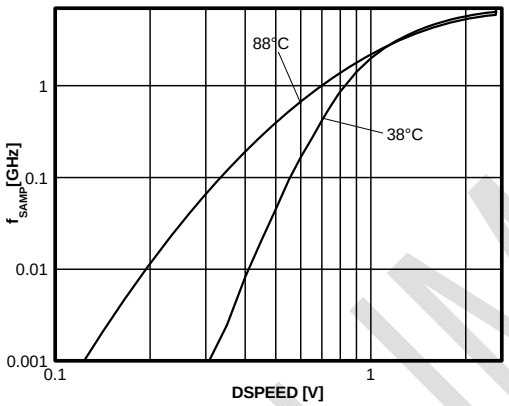
Plot 6. Noise Histogram after offset correction



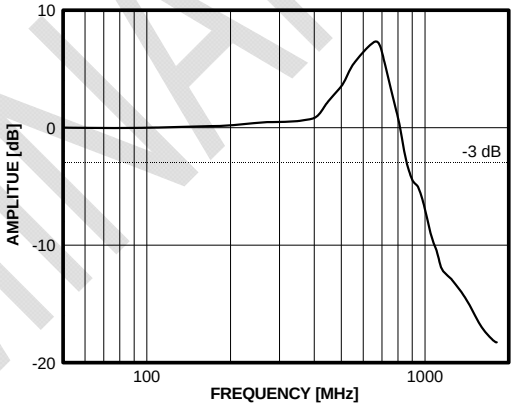
Plot 7. 10 MHz sine wave sampled at 5 GSPS



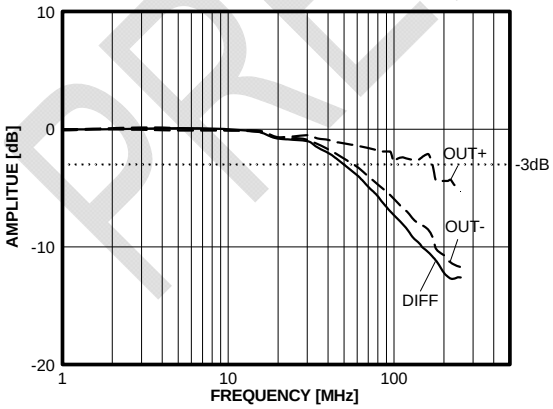
Plot 8. Sampling Speed vs. DSPEED Voltage at 38°C and 88°C



Plot 9. Same as Plot 8 in logarithmic display



Plot 10. Signal Frequency Response[2]



Plot 11. Signal Frequency Response in Transparent Mode

[2] This curve was measured by connecting a Hameg HM8135 3 GHz RF-Synthesizer directly to the DRS4 input. To compensate the cable losses, the signal was measured with a LeCroy WavePro 7300 and a differential WL300 Probe directly at the chip, and the amplitude of the RF-Synthesize was adjusted to keep the amplitude constant over the whole frequency range.

THEORY OF OPERATION

The DRS4 consists of an on-chip inverter chain generating a sampling frequency up to 6 GHz (domino wave circuit), eliminating the need to feed an external sampling clock in the GHz range into the chip. This signal opens write switches in all 9 sampling channels, where the differential input signal is sampled in small (150 fF) capacitors. After being started, the domino wave runs continuously in a circular fashion until de-coupled from the write switches by a trigger signal, which freezes the currently stored signal in the sampling capacitors. The signal is then read out via a read shift register for external digitization.

DOMINO WAVE CIRCUIT

The domino wave circuit is basically a series of 1024 double inverters. After raising the DENABLE signal high, a wave traverses through these inverters producing the write signal for the sampling cells. *Figure 2* shows a simplified schematics of two double inverter blocks.

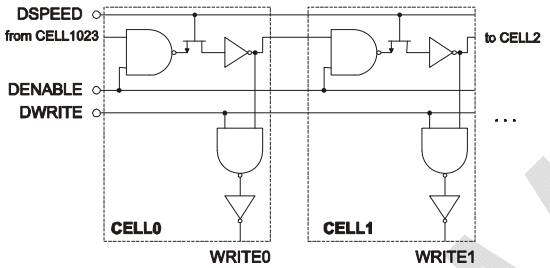


Figure 2. Simplified schematics of two out of 1024 double inverter blocks forming the domino wave circuit

The first inverter is actually an AND gate. This allows to enable and to stop the domino wave at any time via the DENABLE signal. The AND gate is connected to the following inverter via an NMOS transistor operating as a voltage controlled resistor. This resistor forms with the parasitic input capacitance of the inverter a RC-circuit, imposing a variable delay for the propagation of the domino wave, which can be controlled by the analog voltage DSPEED. Since the actual domino wave speed depends on the power supply voltage and the temperature, some stabilization is necessary to ensure steady operation. For this purpose the DTAP signal is available, which toggles its state each time the domino wave reaches cell #512. If operating the chip at f_{DOMINO}, the DTAP outputs a rectangular signal with 50% duty cycle with a frequency according to following formula:

$$f_{DTAP} = \frac{1}{2048} \times f_{DOMINO}$$

The domino wave gets started by raising the DENABLE signal high (see *Figure 3*). An internal circuit ensures that the write signal is always 16 cells wide. If DMODE is high, the domino wave runs infinitely until being stopped by setting DENABLE low. If DMODE is low, the domino wave only propagates once through each cell and stops after cell 1023. In this case only a single low-to-high transition at cell 512 is seen at the DTAP output. The DMODE signal can be controlled through the configuration register (see chapter CONFIGURATION). The DWRITE signal determines if the write signal is sent to the sampling cells. If using the PLL circuit, it might be advantageous to keep the domino wave running also during the readout phase to avoid the time needed for the PLL to lock after each readout. This can be achieved by keeping DENABLE high and only lowering DWRITE to stop the sampling process. In this case, the DTAP signal is also produced by the revolving domino wave during the readout phase. If power minimization is however an issue, the domino wave can be stopped for the readout (dashed line in *Figure 3*). The DWRITE signal must be lowered however before the DENABLE signal for proper chip readout by at least t_{DSTOP}.
If the domino wave is kept running during chip readout, care has to be taken that the DTAP signal does not interfere with the analog output of the DRS4 chip and therefore degrading the signal quality.

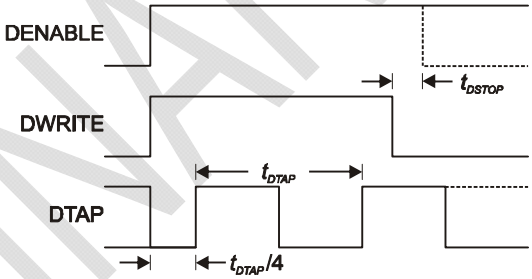


Figure 3. Timing of the Domino Wave Circuit

During power-up, care has to be taken that the DENABLE and DWRITE signals are low. If not, the domino wave can get started before the power supply voltages are stable, which brings the DRS4 chip into a state where it draws a considerable amount of current and heats up significantly. This can be problematic if the signals are directly generated by a FPGA, since most FPGAs have internal pull-up resistors which get activated during the configuration phase of the FPGA. In such a case, the DENABLE and DWRITE signals should be connected to GND with a pull down resistor. This resistor should be much smaller than the FPGA pull-up resistor in order to keep the signals close to GND during the FPGA configuration. A typical value is 4.7 kΩ.

INTERNAL PLL

The DTAP signal can be fed into the internal PLL circuit to lock the domino frequency and phase to a quartz generated reference clock as shown in *Figure 4*. The reference clock has to be equal to the desired f_{DTAP} frequency. To operate the DRS4 chip for example at a 2.048 GHz sampling frequency, the reference clock has to be equal to 1 MHz. To ensure low-jitter operation, the reference clock input uses the LVDS standard. The reference clock can be produced directly by a quartz oscillator. For applications where the frequency should be variable, the clock can be produced by a programmable clock generator. Care has to be taken however that the reference clock signal has a small timing jitter, since it directly affects the sampling jitter of the DRS4 chip. Using a low noise AV_{DD}, a residual PLL jitter of 25 ps can be achieved. The duty cycle of the reference clock is not important for the

functioning of the internal PLL, since it compares the DTAP signal with the reference clock only on the rising edge. For the PLLLCK signal to work correctly, it is however necessary that the duty cycle is close to 50%. If this is not the case, the PLLLCK signal is not reliable, but the locking state of the PLL can still be determined by comparing the reference clock and the DTAP signal externally.
If no LVDS reference clock signal is available, a CMOS signal can be connected to REFCLK+ and the REFCLK- input is connected to VDD/2 via a resistor divider.

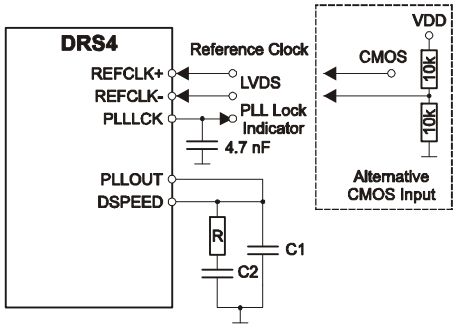


Figure 4. Operation of the internal PLL using an external Loop Filer

For the PLL to work, an external loop filter is required. This filter ensures quick locking and stable operation at the desired sampling frequency. Following table lists typical values for R and C1/C2 for various sampling frequencies:

Table 3. Typical loop filter parameters

Sampling Frequency	R [Ω]	C1 [nF]	C2 [nF]	Lock time [µs]
1 GHz	TBD	TBD	TBD	TBD
2 GHz	TBD	TBD	TBD	TBD
3 GHz	TBD	TBD	TBD	TBD
6 GHz	220	2.2	27	50

The PLL lock indicator is a simple XOR of the DTAP and the REFCLK signals. An external 4.7 nF capacitor to GND integrates this signal, so that a normal CMOS input of a FPGA can be used to determine the lock state. About 10 µs after the PLL has locked, the PLLOUT signal will increase above VDD/2 and indicate the lock.
In case no PLL operation is wanted, the DSPEED input can directly be connected to an external DAC for example and the sampling frequency can be measured using a frequency counter on the DTAP output. In this case the internal PLL should be switched off by setting the PLLEN bit in the configuration register to 0. The maximum samping speed varies from chip to chip between 5.4 GSPS and 6.2 GSPS. The minimal sampling speed is 700 MSPS.

APERTURE JITTER

A small timing jitter is present between the double inverter blocks. This causes the analog input signal to be sampled at time intervals which are not exactly equidistant and therefore causes an aperture jitter. This jitter is composed of a constant deviation for each cell (the so-called “fixed pattern aperture jitter”) arising from the mismatch of the transistors in each cell, and a variable term for each domino revolution (“random aperture jitter”). While the average sampling frequency can be stabilized by using the PLL, a cell-to-cell variation will still be present. If applications require high timing accuracy, the fixed pattern jitter can be calibrated and corrected for. Since one domino wave circuit controls all 9 channels inside the DRS4, only one channel for each DRS4 chip needs to be calibrated. One possibility to do this is to sample a high accurate sine wave with the DRS4 chip, and look for deviations between the sampled waveform and the ideal one obtained from a sine fit of all samples. Averaging over many waveforms at different phases of the sine wave, the fixed pattern aperture jitter can be measured and stored for calibration in a database for example.
An additional complication might arise from the fact that the domino wave can only be stopped between cells. This gives a timing accuracy of $1/f_{DOMINO}$. For applications requiring higher timing accuracy, it is therefore recommended to measure the timing relative to the reference clock and not to the trigger signal. The achievable accuracy is then only determined by the PLL jitter of the DRS4 chip. For even better timing accuracy eliminating the PLL jitter, it is possible to sample a highly stable clock signal or sine wave in channels 8 of each DRS4 chip. By fitting this clock signal event by event, the actually sampling frequency and phase for each waveform can be measured with high precision, and a timing accuracy well below 10 ps can be achieved.

ANALOG INPUTS

Each sampling cell consists of a sampling capacitor with C_s = 150 fF connected to the IN+ and IN- inputs via two NMOS transistors (*Figure 5*). This allows a quasi differential input, given than both input signals do not exceed the rails of the power supply. It has to be insured that the signal source has enough driving capability to deliver the current to charge the capacitors. At 6 GHz sampling speed, an input current of almost 1 mA in necessary to charge the capacitors with a 1 V signal for example. After the sampling cycle, the capacitor stores the voltage

$$U_s = U_{IN+} - U_{IN-}$$

Since the NMOS transistors show a nonlinear behavior when approaching the rails, it is recommended to operate them between 0.1 V and 1.5 V. The common mode of the input signals should therefore be chosen such that none of the input signals is below 0.1V or above 1.5V over the full dynamic range. The range is then limited only by the linearity of the readout buffer in each cell, which shows a non-linearity better than 0.5 mV for an input voltage between 1.05 V and 2.05 V. If differential signals smaller than 1.05 V should be sampled, it is possible to shift U_s up by applying an external voltage ROFS (“read offset”) during the readout phase. This works similar like a charge pump, lifting the bottom plate of the capacitor from IN- to ROFS. The voltage seen by the buffer during readout is therefore

$$U'_S = U_{IN+} - U_{IN-} + U_{ROFS}$$

A differential input range of 0 V to 1 V can therefore be obtained for example by applying 1.05 V to the ROFS input. A differential range of -0.5 V to +0.5 V can be obtained by applying 1.55 V to the ROFS input. The maximal value of the ROFS input is 1.6 V due to the internal NMOS transistor switching this signal. The DRS4 has an additional buffer at each analog output, which then

shifts this output to a range from approximately 0.8 V to 1.8 V. The overall gain of the analog chain is 0.985. The input signal both at the IN+ and the IN- input should not exceed 1.5 V.

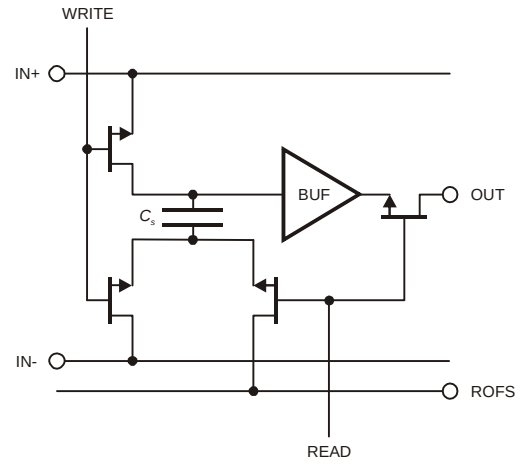


Figure 5. Simplified Schematics of one Sampling Cell

It should be noted that the charge stored in the sampling capacitor is lost over time due to charge leakage, and the readout of a cell should be done quickly (< 1 ms) after the sampling phase.

ANALOG OUTPUTS

The analog outputs OUT+ and OUT- are designed to drive directly the differential inputs of common ADCs. The differentially signaling ensures high noise immunity and requires no additional external components. While the voltage U_+ at the OUT+ output will be in the range from 0.8V to 1.8V (see previous paragraph), the voltage U_- at the OUT- output can be adjusted with U_{ofs} at the O-OFS pin. The relation between these three voltages is given by the following formula:

$$\frac{U_+ + U_-}{2} = U_{ofs}$$

And thus:

$$U_- = 2 \cdot U_{ofs} - U_+$$

The O-OFS pin is internally connected to a weak voltage divider of 16.5 kΩ : 20.3 kΩ which produces approximately 1.37V, and can be overwritten by an externally supplied low impedance voltage source. It can be adjusted such that the dynamic output range of the DRS4 chip matches the dynamic differential input range of the external ADC. If the ADC has for example a differential input range of -1V … +1V, the U_{ofs} voltage should be set to 1.3V. The gives an output range of 1.8V to 0.8V at the OUT- pin according to the above formula and thus a differential voltage of -1V to +1V. The differential gain of the DRS4 chip is then 2, i.e. an input signal with a differential swing of 1V p-p results in a differential output swing of 2V p-p.
To reduce high frequency noise, a low pass filter with a cutoff frequency of half the sampling frequency (Nyquist frequency) of the external ADC can put between the DRS4 outputs and the external ADC inputs.

In the Transparent Mode (see next chapter), the DRS4 input IN+ is directly routed to the output OUT+. In this mode the differential gain is 1, so a 1V differential input signal swing (0.5 V swing at IN+) is seen as a 1V differential output swing signal (0.5 V swing at OUT+).

CONFIGURATION

RESET

To initialize all internal registers to their default value, a negative pulse must be applied to the $\overline{\text{RESET}}$ input with a minimal width of 10 ns. During power up, an internal reset pulse of approx. 1 µs is automatically generated and visible at the reset pin. If during power-up the applied power is unstable for more than 1 µs, an external reset pulse should be applied once the power is stable. Otherwise the pin can just be left open.

REGISTERS

The DRS4 chip has four shift registers which must be accessed for configuration and during readout. To minimize the number of required package pins, a common interface using the SRIN, SRCLK and SROUT signals has been chosen together with an addressing scheme using the address inputs A3-A0. While the SRIN signal is directly connected to all shift registers, the SRCLK is enabled only for a certain shift register if it is addressed. Similarly, the SROUT signal is multiplexed between the outputs of the four shift registers as shown in *Figure 6*.

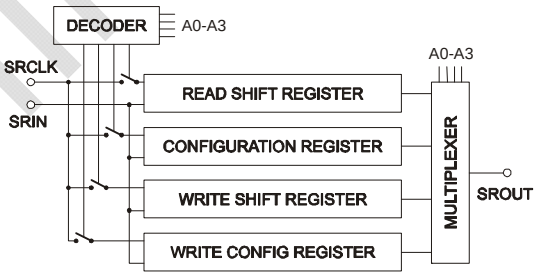


Figure 6. Sharing of Shift Register Signals

In addition to address the shift registers, the address bits A3-A0 are used for various other operations as can be seen in *Table 4*

Table 4. Address Bit Settings

A3	A2	A1	A0	Output
0	0	0	0	Channel 0 at MUXOUT
0	0	0	1	Channel 1 at MUXOUT
0	0	1	0	Channel 2 at MUXOUT
0	0	1	1	Channel 3 at MUXOUT
0	1	0	0	Channel 4 at MUXOUT
0	1	0	1	Channel 5 at MUXOUT
0	1	1	0	Channel 6 at MUXOUT
0	1	1	1	Channel 7 at MUXOUT
1	0	0	0	Channel 8 at MUXOUT
1	0	0	1	Enable OUT0-OUT8
1	0	1	0	Enable Transparent Mode
1	0	1	1	Address Read Shift Register
1	1	0	0	Address Config Register
1	1	0	1	Address Write Shift Register
1	1	1	0	Address Write Config Register
1	1	1	1	Disable all outputs (standby)

The first 9 settings address a single channel for readout through the analog multiplexer, while address 1001_b enables all output buffers for parallel readout as described under WAVEFORM READOUT.

The Configuration Register contains eight bits used to control some behavior of the DRS4 chip, out of which only four are currently used. *Table 5* gives and overview of these bits. After a reset, the default of all bits is 1.

Table 5. Config Register Bit Designations

Bit Location	Bit Mnemonic	Description
Bit0	DMODE	Control Domino Mode. A 1 means continuous cycling, a 0 configures a single shot
Bit1	PLLEN	Enable bit for the PLL. A 1 enables the operation of the internal PLL
Bit2	WSRLOOP	Connect WSRIN internally to WSROUT if set to 1
Bit3-7	Reserved	A 1 must always be written to these bit positions

To write these bits, the timing diagram from *Figure 7* must used: The unused bits must but always be 1.

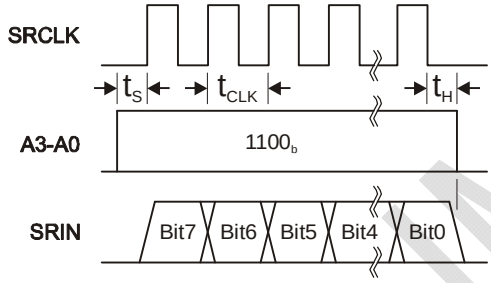


Figure 7. Configuration Register Timing Diagram

The new register content becomes immediately active at the eighth rising edge of the SRCLK signal.

TRANSPARENT MODE

Many applications do not only need fast digitizing of some signals, but also to generate a trigger out of these signals. Traditionally, the signal path is split into a dedicated trigger logic and into waveform digitizing. Using the DRS4 chip, this is not necessary any more. Setting A3-A0 to 1010_b, the analog input to the DRS4 chip is digitized and applied to the analog output at the same time. In this "transparent mode", all nine analog outputs can be digitized with the maximum speed of the external ADC. An attached FPGA can then make a local trigger decision based on the signal of the eight channels. It can apply algorithms such a discrimination or majority logic. When a trigger decision is made, the FPGA stops the DRS4 chip and reads out the high speed sampling data through the same eight ADCs. By using highly integrated octal ADCs such as the AD9222 from Analog Devices or the ADC12EU050 from National Semiconductor, a very compact trigger and digitizing electronics can be built.

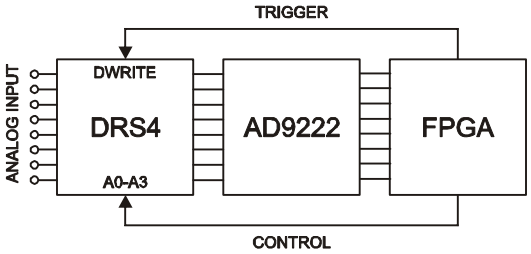


Figure 8. Simultaneous Waveform Digitizing and Triggering using the same ADC

The analog output of the DRS4 chip has been designed to match directly the input of the AD9222. The bandwidth of the DRS4 output buffers is ### MHz, so if the ADC samples at a smaller frequency than twice this bandwidth, some low pass filtering might be required to limit the bandwidth to the Nyquist rate. Alternatively, the OUT+ output can directly be fed into a hardware comparator to trigger if the signal is above a certain threshold.

STANDBY MODE

The DRS4 chip can enter a standby mode by setting A3-A0 to 1111_b. In this mode, all output drivers are disabled and the internal bias generators are switched off to minimize power dissipation. If the domino wave is stopped by setting DENABLE low at the same time, the power consumption is only 50 μW. When exiting the standby mode, the internal bias generators require ### ns for power-up and stable operation.

CASCADING OF CHANNELS

It is possible to cascade two or more channels to obtain deeper sampling depth with the cost of having fewer channels per chip. The sampling cells on DRS4 can be cascaded according to *Table 6*.
A Write Shift Register containing 8 bits is used to activate channel 0 to 7. Channel 8 is always active and can be used to digitize an external reference clock. The bits are shifted by one position on each revolution of the domino wave. If this register is loaded with 1's, all channels are active all the time, and the DRS4 works like having 8 independent channels. The other extreme is a single 1 loaded into the register. This 1 is clocked through all 8 positions consecutively. It then shows up at the WSROUT output and can be fed back into the shift register via the WSRIN input or internally by setting WSRLOOP in the Configuration Register to 1 to form a cyclic operation. This means that on the first domino revolution the first channel is active; on the second domino revolution the second channel is active and so on. If the input signal gets fanned out into each of the 8 channels, the DRS4 chip works like having a single channel with 8 times the sampling depth.

Table 6. Cascading of Channels

Number of channels	Number of sampling cells per channel	Initial Write Shift Register bit pattern
8	1024	11111111_b
4	2048	01010101_b
2	4096	00010001_b
1	8192	00000001_b

To configure the Write Shift Register to one of the above configurations, the bit pattern according to *Table 6* has to

be written into the register initially according to the timing diagram given in *Figure 9*.

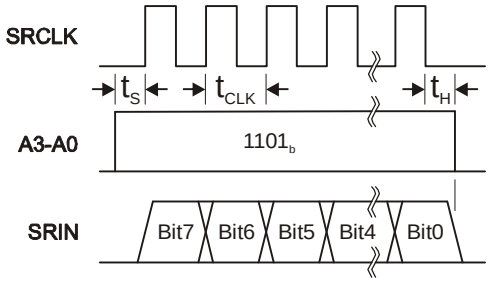


Figure 9. Write Shift Register Timing Diagram

Writing to the shift register is enabled by setting A3-A0 to 1101_b. Eight bits are then clocked into the shift register, MSB first. Bits are latched into the shift register on the falling edge of SRCLK.
After the domino wave has been started via the DENABLE signal, the bit pattern is shifted by one position on each revolution of the domino wave as long as the DENABLE and DWRITE signals are high.

DAISY-CHAINING OF SEVERAL CHIPS

The maximum channel depth of the DRS4 chip is 8192 cells. If deeper sampling depths are required, several DRS4 chips can be daisy-chained. To do so, one has to connect the WSROUT signal to the WSRIN signal of the next chip as shown in *Figure 10*. The first chip is configured for one channel (using the bit pattern 00000001_b) while the Write Shift Register of the second chip is configured to contain all zeros. The same reference clock must be fed into both chips, so that the phase of the domino wave is aligned. During the first eight revolutions of the domino wave the first chip is active. Then the write bit is passed to the second chip, where it will activate the channels for the next eight revolutions. Then it is passed back to the first chip and so on. Note that for this operation the WSRLOOP bit in the Configuration Register has to be set to 0. Using eight DRS4 chips for example, a single sampling channel with a depth of 64k samples is formed. Care must be taken that the signal source is strong enough to drive the capacitive load of all inputs.

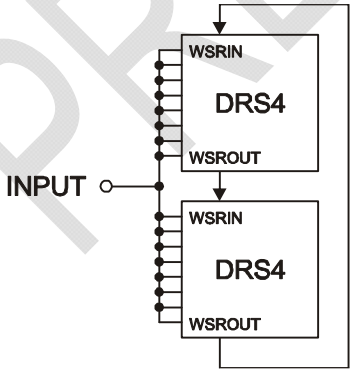


Figure 10. Daisy-Chaining of two DRS4 Chips

WAVEFORM READOUT

After sampling has been stopped by either setting DENABLE or DWRITE low, the waveform can be read out via the read shift register. There are two possible modes for readout. The "full" mode reads all 1024 cells, while a special Region-Of-Interest mode only reads a certain window of the waveform to reduce dead time. The contents of the 9 DRS4 channels can either be digitized with a single external ADC using the internal multiplexer, or with eight external ADCs in parallel to reduce dead time.

FULL READOUT MODE

In the full readout mode, all 1024 sampling cells are read out consecutively starting from cell 0 with 1024 clock cycles at 33 MHz. Care has to be taken in the PCB design that the DENABLE, DWRITE and DTAP signals are well shielded from the analog signals. Otherwise some crosstalk between these signals and the data channels may occur, as can be seen in *Plot 4*.

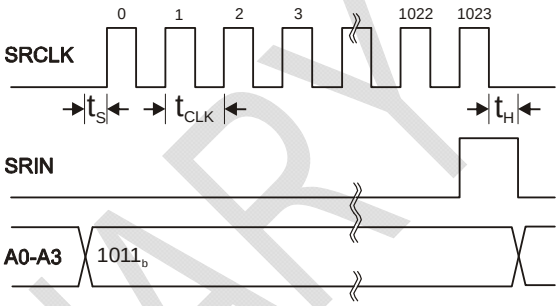


Figure 11. Read Shift Register Initialization

To start the full readout mode, the Read Shift Register has to be initialized by clocking a "1" into the first cell. This is achieved by applying address 1011_b at the address input A3-A0 and issuing 1024 clock cycles of SRCLK, where only during the last one SRIN=1 is applied (*Figure 11*). After initialization, each channel can be read out following the diagram of *Figure 12*.

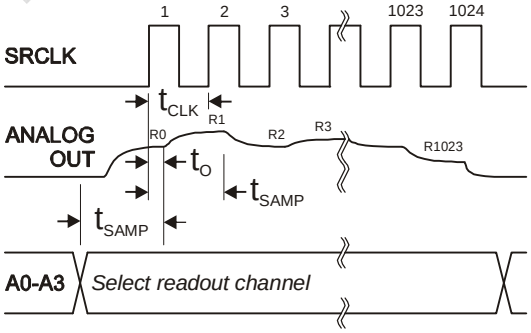


Figure 12. Full Readout Mode Timing Diagram

The address of the channel which should be read out should be applied to A3-A0. This reveals the first cell contents at the analog output MUXOUT, which should be digitized after t_{SAMP}. Then the "read bit" is shifted down on each consecutive clock cycle of SRCLK, until it reaches cell 1023. One more clock cycle should be applied (noted "1024" in *Figure 12*) to wrap around the read bit into cell #0, so the next channel is ready for readout. On the rising edge of SRCLK at each clock cycle the contents of the next sampling cell appears at the analog output MUXOUT after a delay of t_O = 10 ns if the multiplexer is used. When operated at 33 MHz clock speed (t_{CLK} = 30 ns), the analog signal has 30 ns to settle at the output. Care must be taken to sample it with an external ADC at the end of this 30 ns period, but just before the beginning of the next cycle. So with $t_{SAMP} = t_O + t_{CLK}$ = 40 ns the sampling should occur about

38 ns after the rising edge of SRCLK. Sampling the signal after 35 ns already degrades the DRS4 linearity. Since each sampling cell contains an internal buffer, an offset error from that buffer is seen due to the mismatch of the transistors inside the buffer, which is typically 5 mV rms (*Plot 3*, *Plot 5*). Since this offset error is constant over time ("fixed pattern noise"), it can be measured and corrected for during the readout. One example to do this is to put an offset correction table into the FPGA which does the readout of the ADC connected to the DRS4. This way the noise can be reduced by more than one order of magnitude. Care has to be taken to choose an ADC which matches the performance of the DRS4. Many 12-bit ADCs have a SNR which is lower than 70 dB and would therefore not give optimal performance.

CHANNEL MULTIPLEXER

Four address bits A3-A0 are used to configure the analog output. In multiplexed mode, each channel's analog output can be routed to one single output MUXOUT, making it possible to use only a single external ADC to digitize all 9 channels. Please refer to *Table 4* for the addressing scheme. If digitization time however is important, all 9 channels can be digitized in parallel using 9 external ADCs, thus reducing the digitization time by a factor of 9.

REGION-OF-INTEREST READOUT MODE

The digitization of all 1024 samples at 33 MHz takes 30 µs, even if the 9 channels are digitized in parallel. During this time the sampling of the DRS4 is stopped and no new waveforms can be acquired. To reduce this dead time, it is possible to read only a subset of all sampling cells, for applications where one is interested only in short pulses like illustrated in *Figure 13*.

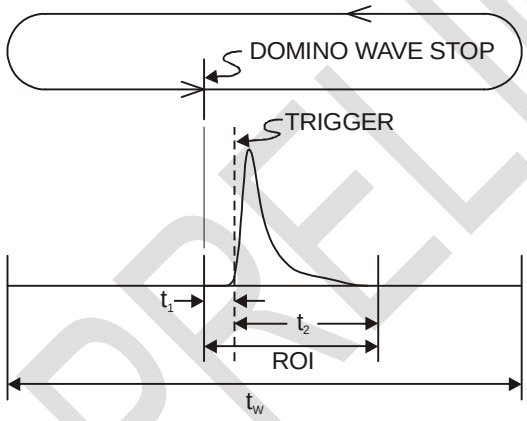


Figure 13. Region-of-Interest (ROI) Readout Mode

Assume that the domino wave is running with a window size $t_W = 1/f_{SAMP} \times 1024$, and a short signal occurs, like a hit from a photomultiplier. This signal triggers an external trigger circuit, similar like in an oscilloscope. The interesting part of the waveform is now in a region t_1 before and t_2 after that trigger point. If only this ROI is read out, the dead time will be reduced by the fraction $(t_1+t_2)/t_W$. To achieve this with DRS4, the domino wave has to be stopped t_W-t_1 after the trigger by means of an external delay. If the trigger has already a latency of t_t, then a fixed delay $t_f = (t_W-t_1)-t_t$ must be added to the trigger. The stop position of the domino wave is then transferred into the readout shift register via a pulse on the RSRLOAD pin. The readout starts at this position and can be stopped by the readout FPGA firmware after *n* samples when the complete ROI is covered. *Figure 14* shows the timing for this readout mode.

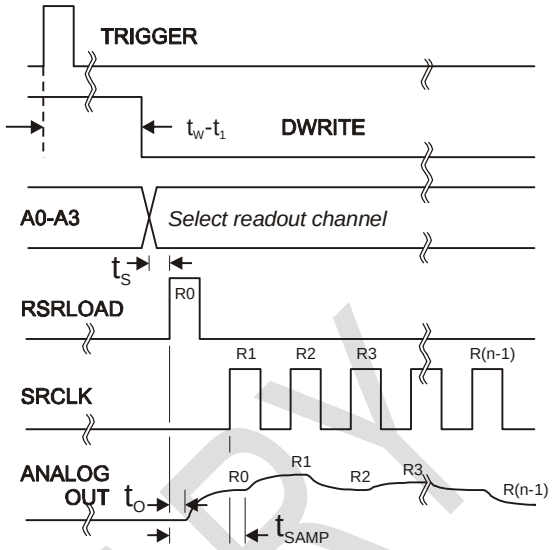


Figure 14. ROI Readout Mode Timing Diagram

The rising edge of the RSRLOAD pin transfers the first sample R0 of the ROI to the analog output, where it can be digitized after (t_{SAMP}.- 2ns). Consecutive pulses on SRCLK transfer the following samples R*i*, until all *n* samples are digitized. This sequence can be repeated 9 times to digitize all channels if multiplexing is used. Each pulse on RSRLOAD re-transfers the domino wave stop position into the read shift register, so the same ROI can be digitized on all channels. If the read bit arrives at cell #1023, it wraps around automatically into cell #0.
If offset correction is applied during readout, one hast to know which cell is currently visible at the analog output, since each cell has a different offset value. Using the ROI readout mode, the first cell to be read out can be any of the 1024 cells. To determine the cell number where the sampling has been stopped, the stop shift register can be used. It stores the cell number where the sampling has been stopped and encodes this position in a 10 bit binary number ranging from 0 to 1023. This encoded position is clocked out to SROUT on the first ten readout clock cycles, as can be seen in *Figure 15*. The rising edge of the RSRLOAD signal outputs the MSB, while the falling edges of the SRCLK signal reveal the following bits up to the LSB.

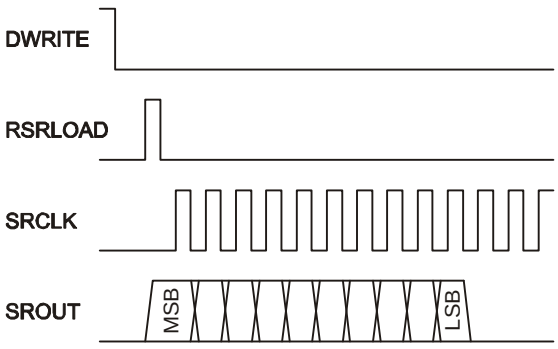


Figure 15. Stop Shift Register Timing Diagram

If the DRS4 is configured for channel cascading or daisy-chaining, it is necessary to know which the current channel is where the sampling has been stopped. This can be determined by addressing the Write Shift Register with

A3-A0 = 1101_b and by applying clock pulses to the SRCLK input. If the DRS4 is configured in single channel mode and the sampling stopped at channel *i*, then 8-*i* clock pulses will reveal the 1 at the WSROUT and the SROUT outputs.

SIMULTANEOUS WRITING AND READING

With the DRS4 chip it is possible to sample the input with one channel while reading out another channel at the same time, with the drawback of slightly increased noise. This mode can be used to build a system with up to eight parallel analog buffers and with virtually zero dead time for event rates below the typical readout time. To do so, a layout similar to the one from the channel cascading is used. A single input channel is distributed to some or all DRS4 inputs. The write shift register is however not advanced by the domino wave revolution, but under the control of the FPGA. For this purpose a second write shift register, called the Write Config Register, has been implemented. A sampling channel is active only if both the Write Shift Register and the Write Config Register contain a 1. Following flow is used for example for a system where a signal is connected to all eight DRS4 channels:

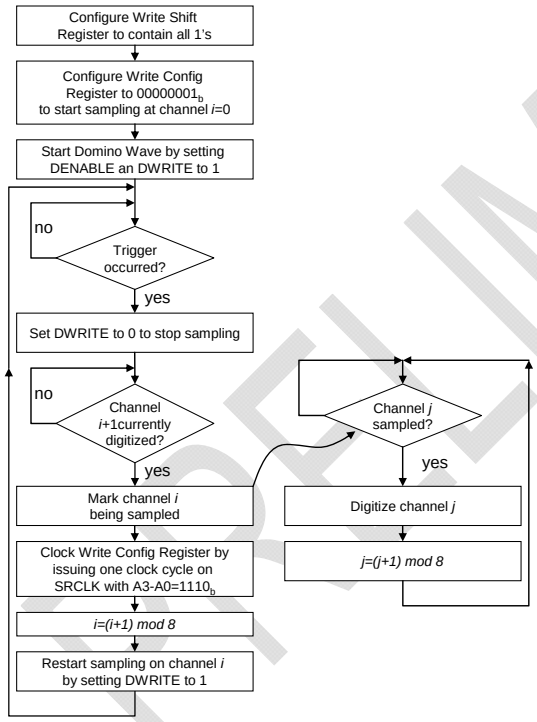


Figure 16. Flow for concurrent sampling and digitizing

Two concurrent threads of operation have to be implemented typically in an FPGA. One thread (shown at the left side) waits for a trigger and re-arms the DRS4 chip sampling on the next channel. This operation can be done very quickly in just a couple of FPGA clock cycles of typically 100 ns in total and is then the only contribution to the dead time. The second thread (shown at the right side) waits for a channel to be marked as sampled by the first thread and then starts the digitization. If there is one or more other triggers happening during this digitization, the first thread will "pause" the readout thread (since both threads share the same A3-A0 address lines), advance the sampling channel by one each time, then resume the readout thread. In this way, up to eight analog sampling buffers can be filled before the sampling will be blocked. Depending on the rate and time distribution of the triggers, the overall dead time will be reduced dramatically by using this scheme.

If it is required to use simultaneous writing and reading together with channel cascading, the techniques from the sections CASCASING OF CHANNELS and SIMULTANEOUS WRITING AND READING have to be used together. If the DRS4 is configured for four channels with 2048 bins for example, the number of analog buffers will be reduced from eight as above to four. The cascading of the channel pairs is controlled by the domino wave and the Write Shift Register, while the channel selection for sampling is controlled by the Write Configuration Register. In this case this register contains an initial value of 00000011_b to enable the first two channels to form a single 2048 bin deep channel. After the first trigger, two clock pulses must be applied to change this to 00001100_b to enable the next pair of channels and so on.

TYPICAL MODE OF OPERATION

Figure 17 shows the typical mode of operation. The DRS4 chip is connected to a single external ADC and a FPGA. The analog inputs are converted from single-ended to differentially for optimal performance by means of a RF transformer. The PCB has to be designed carefully to minimize the cross-talk between the different channels. A passive interface as shown will reduce the analog bandwidth of the DRS4 significantly (typically to 200 MHz). A higher bandwidth can be achieved with an active differential high speed buffer at the DRS4 input. Channel 8 can be used to digitize an external LVDS master clock for applications where precision timing is required for many DRS4 chips. The reference clock to stabilize the Domino Wave is generated by the FPGA. By using an internal clock manager or a programmable divider, a wide range of sampling frequencies can be achieved. The values for R and C of the PLL Loop Filter can be obtained from Table 3. The ROFS input can shift the sampled signal into the linear range of the DRS4 chip as described under ANALOG INPUTS. Since a fast low impedance source is required at the ROFS input, a fast buffer must be used as indicated. For maximum flexibility a DAC controlled by the FPGA can be used instead of the potentiometer.

All nine channels are read out through the multiplexer at output MUX/OUT0, as selected by the address lines A0-A3. To reduce the dead time, all eight or nine channels can be digitized in parallel by using an external octal ADC.

The pull-down resistors at the DENABLE and DWRITE lines ensure proper start-up of the chip as described under DOMINO WAVE CIRCUIT.

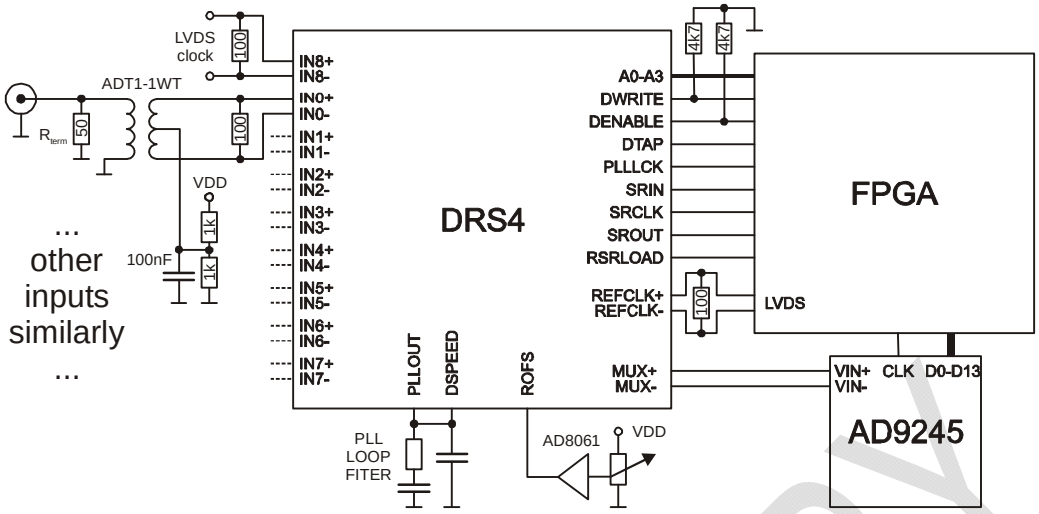


Figure 17. Typical Mode of Operation

OUTLINE DIMENSIONS

76-lead quad flat non-leaded package (QFN)