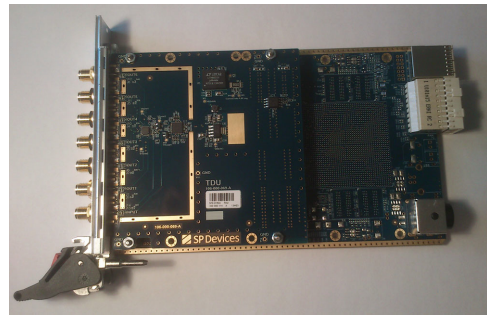


ADQTDU

ADQTDU is a trigger and clock distribution unit for ADQ series of digitizer. The ADQTDU is available in several variants for different types of electrical signaling. The ADQTDU is also available in several form factors for integration different types of systems.



Introduction

The ADQTDU is a fan out buffer with 1 input and 6 outputs. The unit is used for trigger and clock distribution. See **Figure 1** for block diagram.

The ADQTDU is available with several options for logic levels, form factor, and control possibilities.

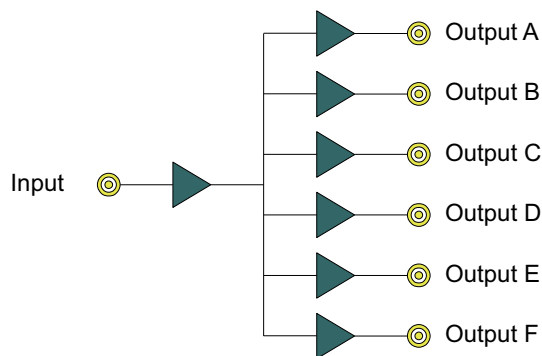


Figure 1: Block diagram of ADQTDU

TECHNICAL DATA ¹	
Number of inputs	1
Number of outputs	6
Power supply	12 V
Power consumption	3 W
Box size	103 x 166 x 31 mm ³
Card size cPCIe/PXIe	1 slot 3U
Card size Micro-TCA	Double width, mid size
Connector	SMA

1. All values are typical unless otherwise noted.

Applications

The LVPECL configuration is ideal for driving clock or clock reference for several ADQ series digitizers.

The LVCMOS configuration is ideal for distributing the trigger to several ADQ series of digitizers.

Ordering information

ORDERING INFORMATION	
ADQTDU	ADQTDU
AVAILABLE OPTIONS	
CMOS	-C
LVPECL	-P
AC LVPECL	-AC
Control function	-CTRL
Stand alone box	-USB
cPCIe/PXIe	-PXIe
cPCIe/PXIe	-MTCA

Example: ADQTDU-P-PXIe

CMOS options

The input is available as logic compatible comparator input and may be driven by TTL, CMOS, etc. The input is 50 Ohms terminated to ground to avoid reflections in cables. Due to the termination to ground, the threshold level is set to the level 0.7 V.

The output are short circuit protected CMOS compatible drivers.

CMOS			
Vth	Input threshold	0.7	V
Rin	Input impedance	50	Ohm
ViH	Input level High (min)	1.1	V
ViL	Input level Low (max)	0.3	V
VoH	Output level High (min)	2.5	V
VoL	Output level Low (max)	0.5	V
Rout	Output impedance	35	Ohms
	Output slew rate	5	V/ns
	Channel–channel skew	50	ps
	Propagation delay	2	ns
	Max frequency	200	MHz
	Additive jitter	250	fs

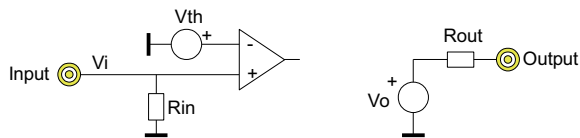


Figure 2: Equivalent circuit diagrams CMOS

Order code: -C

LVPECL option

The ADQTDU also available as single ended LVPECL.

DC COUPLED LVPECL			
Vref	Reference voltage	1.3	V
Rin	Input impedance	50	Ohm
Vi	Input signal	0.5	Vpp
Vo	Output signal	0.6	V
Rout	Output impedance	180	Ohms
	Channel–channel skew	30	ps
	Propagation delay	220	ps
	Max frequency	2	GHz
	Additive jitter	75	fs

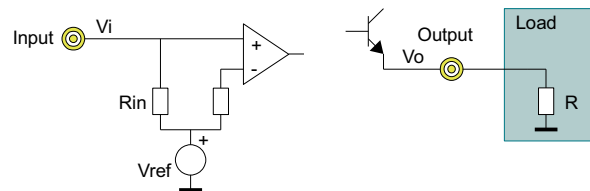


Figure 3: Equivalent circuit diagrams LVPECL

Order code: -P

AC coupled option

The LVPECL version is available for AC coupled systems. This is intended for clock distribution, where the signal is periodic.

The input is AC coupled an AC terminated 50 Ohms. Lower cut of frequency is 10 kHz.

The output has load resistors and is intended to drive AC coupled inputs.

AC COUPLED LVPECL			
RDC	Input impedance DC	10k	Ohm
Rin	Input impedance AC	50	Ohm
Vi	Input signal	0.5	Vpp
Vo	Output signal	TBD	V
Rout	Output impedance	180	Ohms
	Channel-channel skew	30	ps
	Propagation delay	220	ps
	Max frequency	2	GHz
	Additive jitter	75	fs

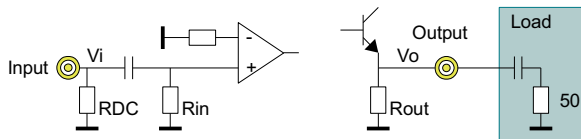


Figure 4: Equivalent circuit diagrams AC LCVPECL

Order code: **-AC**

Form factor option

The ADQTDU is available in various form factors; stand alone box, cPCIe/PXIe, PCIe, and M-TCA.4.

The unit is available in a stand alone box. The box is supplied by an external 12 V power adapter.



Figure 5: Typical box version

Order code: **-USB**

The ADQTDU is available in cPCIe/PXIe form factor. It uses only power supply from the chassis.

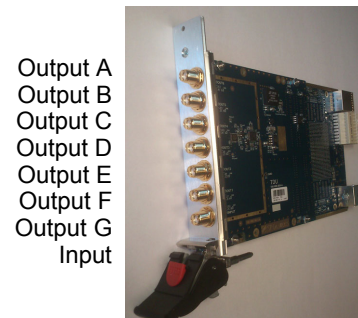


Figure 6: ADQTDU-PXIe form factor

Order code: **-PXIe**

The ADQTDU is available in Micro-TCA form factor. It uses only power supply from the chassis.



Figure 7: Typical MicroTCA version

Order code: **-MTCA**

Controlling the output

The CMOS version is available with a controller interface to turn off the trigger signal. Through an API command, the outputs may be set at high or low. On command, the signal is turned on again. This enable signal may also come from an external input. The enable signal is available at an output for a chain connection of units.

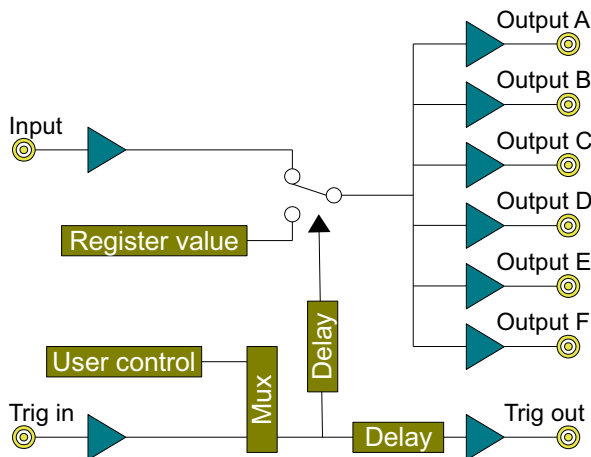


Figure 8: Block diagram of ADQTDU

This function is intended for systems where the trigger signal source is free running and may not be stopped. The sequence of operation is then

1. Set the trigger signal to low
2. Set up all digitizers
3. Send trigger arm command to each of them
4. Turn on the trigger signal

The digitizers will then start simultaneously on the same trigger.

By setting the delay lines, several ADQTDU can be controlled in phase by the same signal, **Figure 9**.

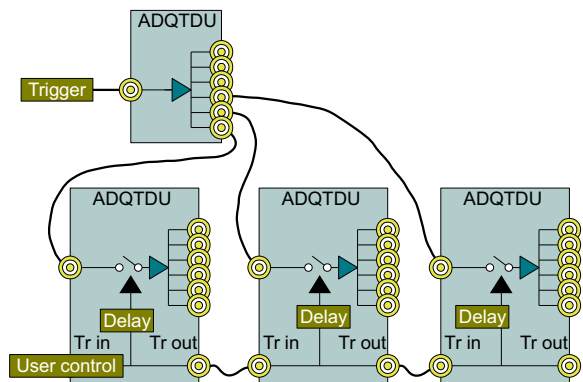


Figure 9: Chain of control for ADQTDU

Order code: -CTRL