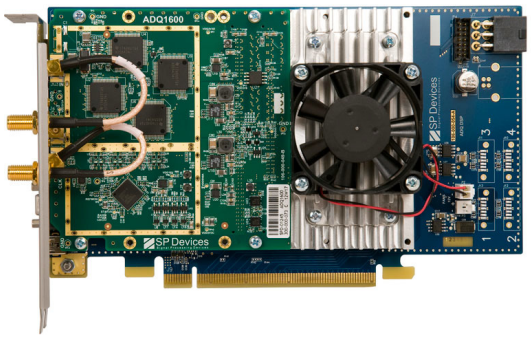

Application Note: Trigger

The trigger block in the ADQ has several configuration options. This application note describes the different triggering functions that are available, and how they should be configured. The differences and similarities between ADQ V5 and ADQ V6 digitizers are highlighted.

Introduction

The trigger function is essential for the digitizer. Trigger is a timing signal from external equipment to activate the digitizer. The trigger may also be generated by the digitizer. It is used for, for example;

- Synchronize the acquisition to external equipment
- Synchronize the acquisition to external activities
- Synchronize the acquisition to signal activity
- Synchronize several digitizers
- Set a real time marker on the captured data
- Control external equipment by trigger generation

The trigger block has a large combination of setting, which are used for getting required functions. The intention is to describe the fundamental settings, which may be combined for huge flexibility.

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Table of Contents

1 Digitizer families

The digitizer families ADQ V5 and ADQ V6 share the same trigger concept and the majority of the functions are the same. The most of the description of the trigger is thus common for ADQ V6 and ADQ V5. However, since there are two hardware platforms, there are also some differences which are highlighted in the appropriate sections.

1.1 Trigger block in ADQ V5 digitizer family

The trigger block is located in FPGA #2 on ADQ V5 digitizer family and handles all trigger events, trigger outputs and other functions concerning the triggering of data acquisitions, **Figure 1**. The trigger is also transmitted to FPGA#1 for usage there (for instance for the waveform averaging function). The separation into 2 FPGAs puts some restrictions on the the trigger flexibility.

The trigger input and output on the digitizer share the same physical connector, which can be used for broadcasting triggers, “EXT TRIG” in **Figure 1**.

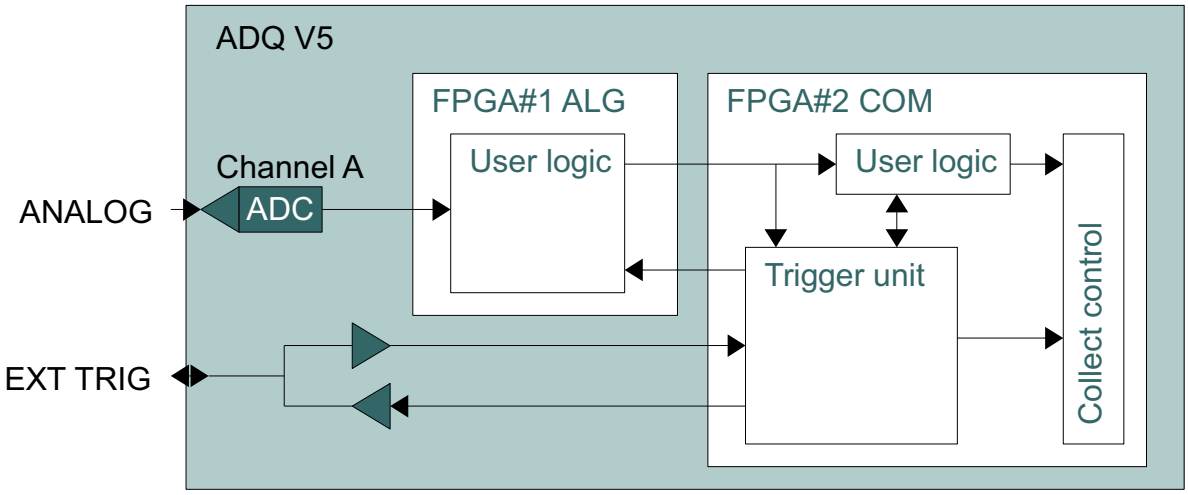


Figure 1: Trigger block in ADQ V5 digitizer family.

1.2 Trigger block in ADQ V6 digitizer family

On the ADQ V6 digitizer family, the trigger function is located in the only FPGA, **Figure 2**. The communication with other functions is thus more straight forward than in the ADQ V5 family. The trigger input and trigger output are on two different connectors, which allows for larger flexibility.

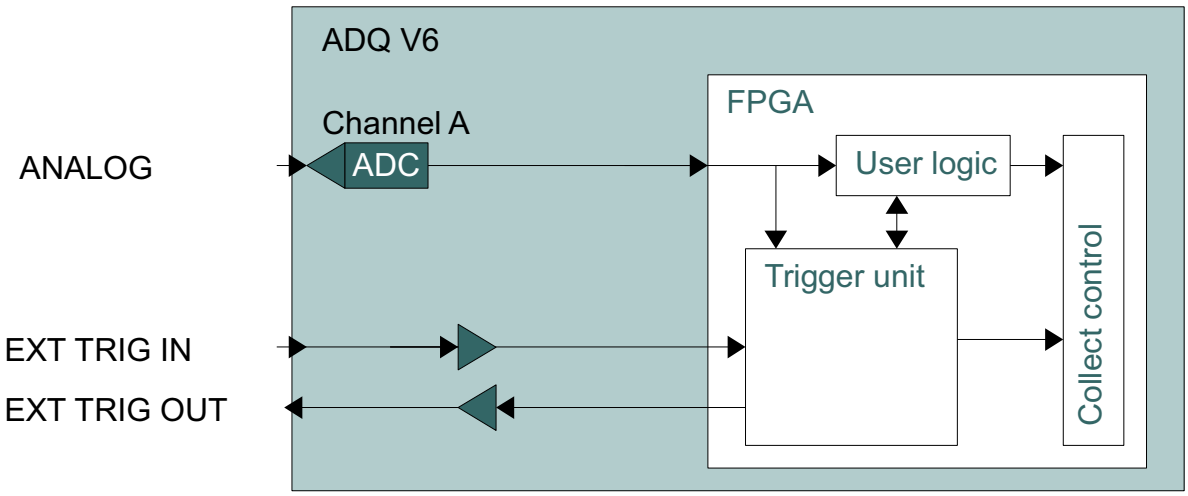


Figure 2: Trigger block in ADQ V5 digitizer family.

1.3 Acquisition modes

The acquisition is possible in two different modes of operation; triggered streaming and multi-record. Both are controlled by the trigger.

- The triggered streaming is optimized for data transfer to host computer.
- The multi record mode is optimized for real time capture of large amount of data.

The triggers support both acquisition modes. More about acquisition modes in the data transfer application note 13-0937.

1.4 Clock base

The clock for the trigger block is derived from the data clock of the ADCs. This is to maintain synchronization with the sampling process. Since different models have different sample rate, the time base in the trigger block will be model dependent.

The clock method is optimized for building synchronous systems, that is, the trigger source is phase locked to the digitizer[1].

On some models, there is a trig time extended accuracy, which allows for sub sample precision on the trigger.

1. Since the trigger is intended for synchronous systems, there is no need for a trigger time interpolating circuit.

1.5 Block diagrams

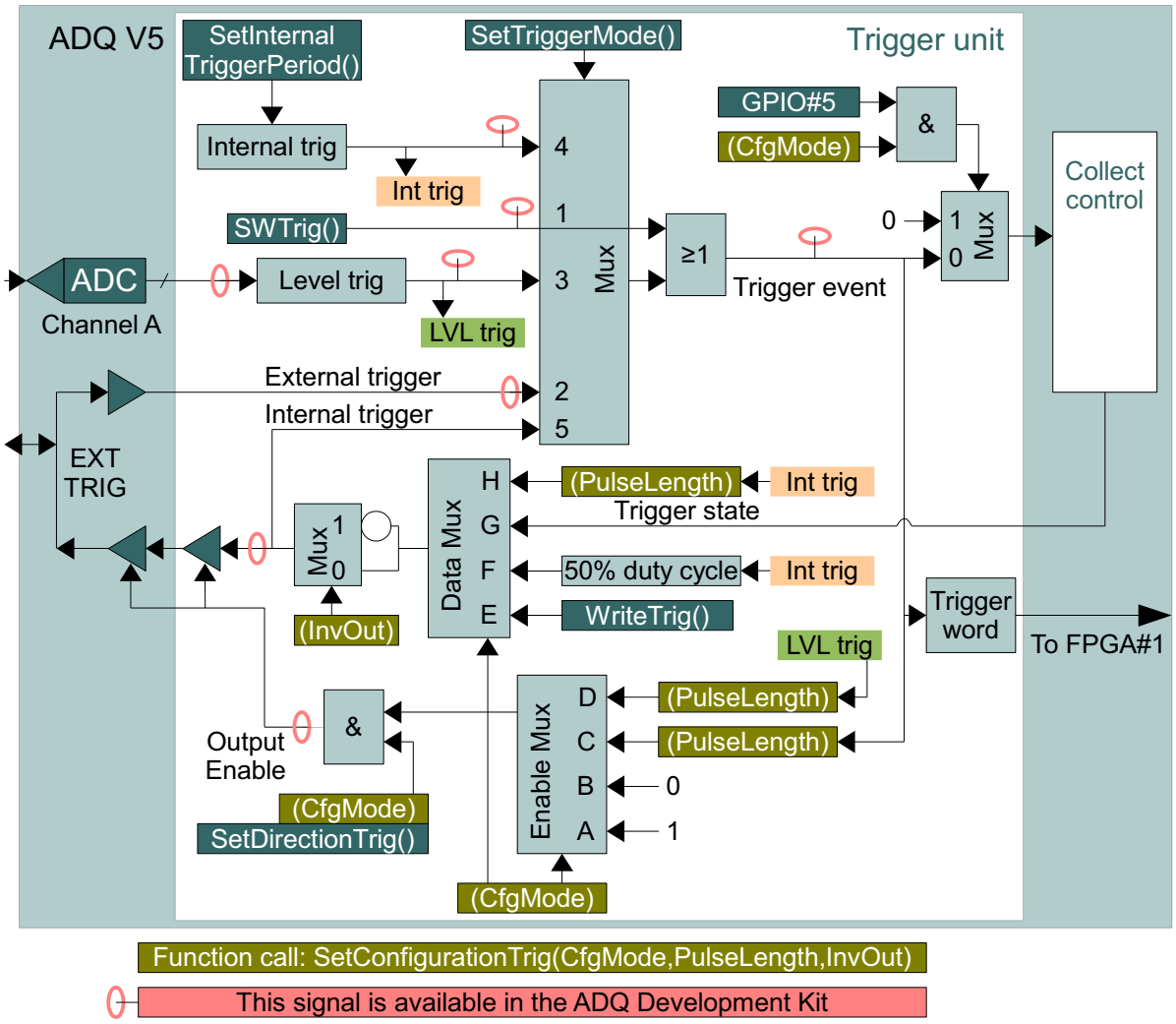


Figure 3: Trigger in ADQ V5

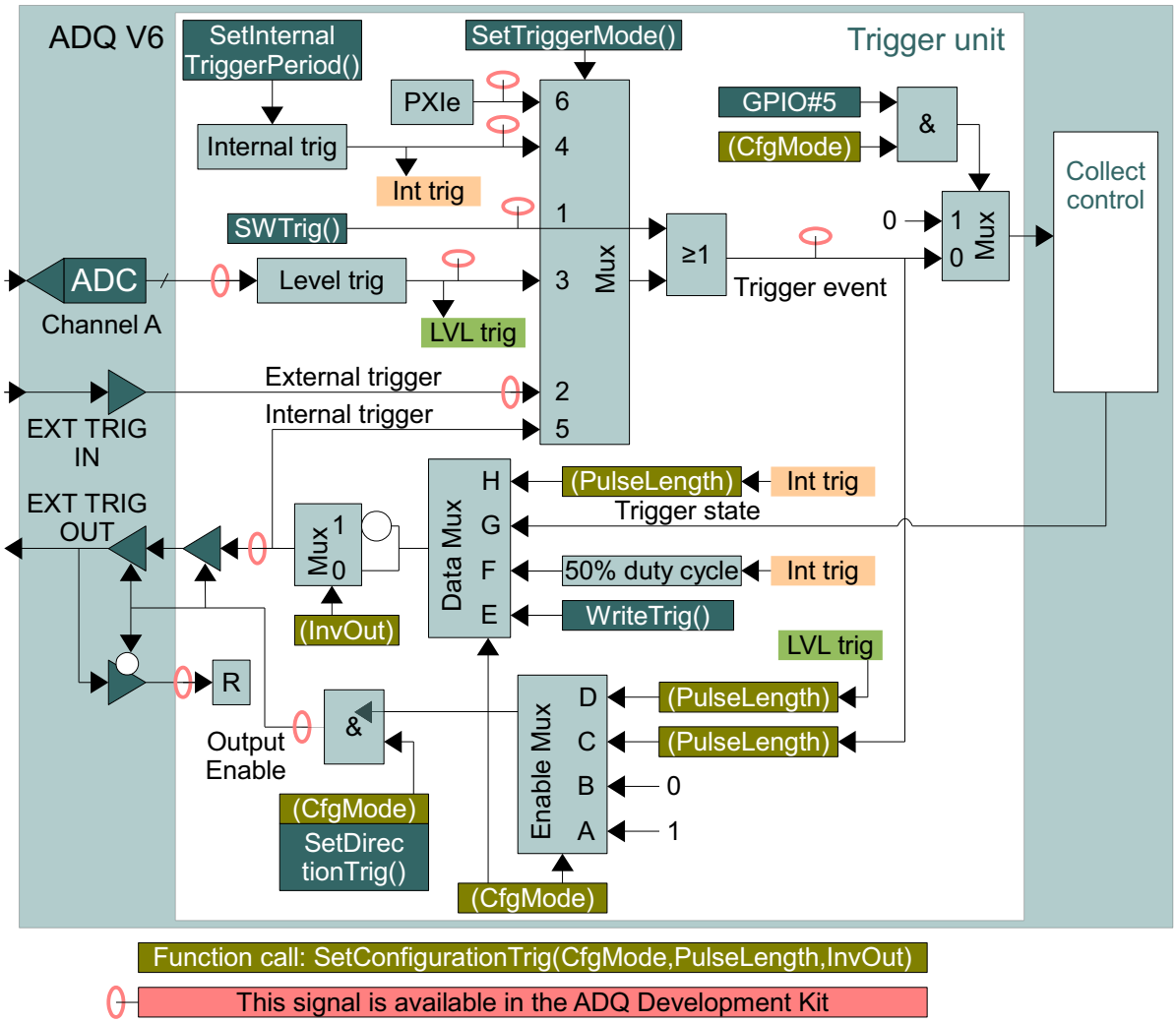


Figure 4: Trigger in ADQ V6

1.6 Trigger related API commands

A short list of the trigger related commands are in **Table 1**. For a complete list, see ADQ API user's guide.

API COMMAND	DESCRIPTION	REFERENCE
SetTriggerMode()	Select accepted trigger(s)	**Section 1.8**
SetDirectionTrig()	Enable trigger output. See also SetConfigurationTrig.	**Section 1.7**
WriteTrig()	Set data on trigger output register (high or low)	**Section 1.7**
SetConfigurationTrig()	Set up trigger output and trigger broadcasting.	**Section 1.7**
SWTrig()	Trigger the device with a software trigger	**Section 2.1**
SetInternalTriggerPeriod()	Sets up the period for the internal trigger	**Section 2.4**
SetPreTrigSamples()	Sets the number of pre-trigger samples	**Section 3.1**
SetTriggerHoldOffSamples()	Sets the trigger delay samples	**Section 3.2**
SetTrigLevelResetValue()	Sets the sensitivity of the level trigger	**Section 2.2**
SetLvlTrigLevel()	Sets the code level for the level trigger	**Section 2.2**
SetLvlTrigEdge()	Configure the level trigger for rising or falling edges	**Section 2.2**
SetLvlTrigChannel()	Configure which channel to level trig on	**Section 2.2**
SetExternTrigEdge()	Configure external trigger for rising or falling edges	**Section 2.3**
SetExternalTriggerDelay()	Adjust the external trigger latency	**Section 3.3**

Table 1: List of trigger commands. See ADQ API user's guide for a complete list

1.7 Trigger output control reference table

Table 2 lists the function call to SetConfigurationTrig() and refer to **Figure 4**. The parameter CfgMode controls the trigger output set up and the input trigger blocking function on GPIO#5. The parameter PulseLength is the pulse length for some funcitons as indicated in **Table 2** and **Figure 4**. The parameter InvOut is inverting the trigger output.

It is not necessary to use the command SetDirectionTrig() when using SetConfigurationTrig().

The command WriteTrig() sets the content of the hardware register bit for the Register trigger.

CFGMODE	PULSE LENGTH	TRIGGER OUTPUT DESCRIPTION	REQUIRES WRITETRIG()[1]	MUX SETTING DATA	OE	REF.
GPIO #5 blocker disabled						
0x00	–	Trigger output disabled. Default.	–	E	A	
0x11	Value	Trigger event	Set to 1	E	C	**Section 4.4**
0x19	Value	Level trigger event	Set to 1	E	D	**Section 4.3**
0x01	–	Register trigger output	Value	E	A	**Section 4.1**
0x41	–	Internal trigger 50% duty-cycle	–	F	A	**Section 4.5**
0x05	–	Trigger state	–	G	A	**Section 4.2**
0x45	Value	Internal trigger	–	H	A	**Section 4.5**
GPIO #5 blocker enabled						**Section 6.1**
0x20	–	Trigger output disabled.	–	E	A	
0x31	Value	Trigger event (PL) WriteTrig(1)	Set to 1	E	C	**Section 4.4**
0x39	Value	LVL trig event (PL) WriteTrig(1)	Set to 1	E	D	**Section 4.3**
0x21	–	Register trigger output	Value	E	A	**Section 4.1**
0x61	–	Internal trigger 50% duty-cycle	–	F	A	**Section 4.5**
0x25	–	Trigger state	–	G	A	**Section 4.2**
0x65	Value	Internal trigger	–	H	A	**Section 4.5**

Table 2: Output selection by SetConfigurationTrig(CfgMode,PulseLength,InvOut)

1. WriteTrig(1) means that the data out bit has to be set with WriteTrig() command for the function to operate.

1.8 Trigger input control reference table

MODE	TRIGGER INPUT DESCRIPTION	REFERENCE
0	Software trigger (default)[1]	
1	Software trigger	**Section 2.1**
2	External trigger	**Section 2.3**
3	Level	**Section 2.2**
4	Internal trigger	**Section 2.4**
5	Trigger output	**Section 2.5**
6	Star trigger PXIe	**Section 2.6**

Table 3: Input selection by SetTriggerMode parameter

1. Software trigger is always active

2 Input triggers

2.1 Software trigger

Software trigger is triggering through the API. Over the API (USB or PCIe link) the trigger is sent to the unit. The exact timing on this trigger is not defined. However it is aligned to the trigger unit clock.

A software trigger is always accepted. This can be used for making time out functions in the applications software. This means that SetTriggerMode(Mode=1) is always active.

2.2 Level trigger

Level trigger is a data path trigger. The sampled data is compared to a specified level and detected on rising or falling edges of this level. The level trigger point out the first sample that is equal or greater than the trigger level for a rising edge. (The first sample that is equal or lower for a falling edge.)

The level trigger has noise suppression function which is controlled by SetTrigLevelReset-Value(). The level trigger detects a rising (or falling) edge on the signal. In presence of high noise, a false detection is possible, **Figure 5**. The trigger reset level is a discriminator that determines a certain trend on the signal for a level trigger detection. The signal has to pass the trigger reset level before a trigger may be activated. The trigger reset point is the first sample below or equal to the trigger reset level. (For falling edge, it is the first sample above or equal to trigger reset level.) The difference between trigger reset level and trigger level represents a signal to noise ratio. A large difference gives high noise immunity. However, a high value also reduces the sensitivity in the measurement system. The value of the trigger reset level has to be adjusted to the present measurement situation.

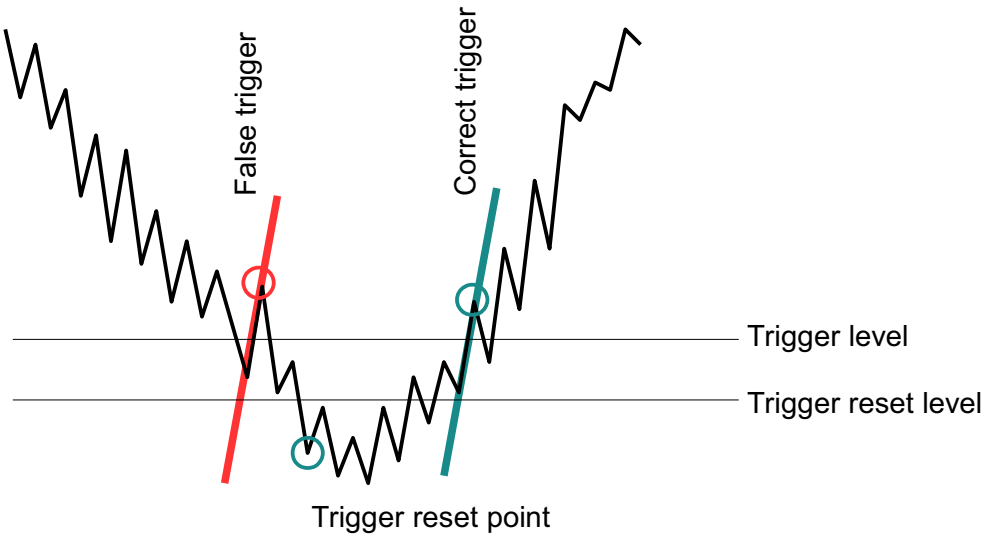


Figure 5: Trigger reset level.

2.3 External trigger

External trigger is the trigger signal physically connected to the digitizer TRIG IN port (TRIG on ADQ V5). External trigger level is determined by a fixed comparator level. The trigger may be configured to trigger on rising or falling edges.

Typically the external trigger timing accuracy is per sample. On some models, a subsample trigger accuracy is available. See **Section 8** on how to use the extra trigger information.

Inside the FGPA, there is a latency on the external trigger compared to the data path. This is adjusted for standard firmware. However, when building custom firmware using the ADQ

Development Kit, this delay may change. There is built in hardware support for adjusting the trigger latency by a software command, **Section 3.3**.

2.4 Internal trigger

The internal trigger generator is an internal counter that generates a periodic trigger. The trigger pulse is available for triggering the digitizer. It is also available at the trigger output. The output trigger pulse length can be either a 50% duty-cycle pulse or a configurable pulse length. The length of the trigger pulse is set as a number of samples.

2.5 Generated trigger

The trigger output function can be used as trigger for the device in itself. This is done by feeding back the trigger output to the trigger input multiplexer. See **Section 4** for more information on trigger output functions.

2.6 PXIe star trigger (ADQ V6)

The ADQ V6 Digitizer family supports star trigger DSTARB and DSTARC for the PXI Express version of the digitizer. See specification of the chassis for availability of these trigger signals.

3 Acquisition control settings

3.1 Pre-trigger

The pre-trigger makes it possible to acquire data before the trigger event, see **Figure 6**. The size of pre-trigger depends on acquisition mode. For streaming mode, the size of the pre-trigger is limited, whereas for the multi-record mode it can be up to 2^{34} samples.

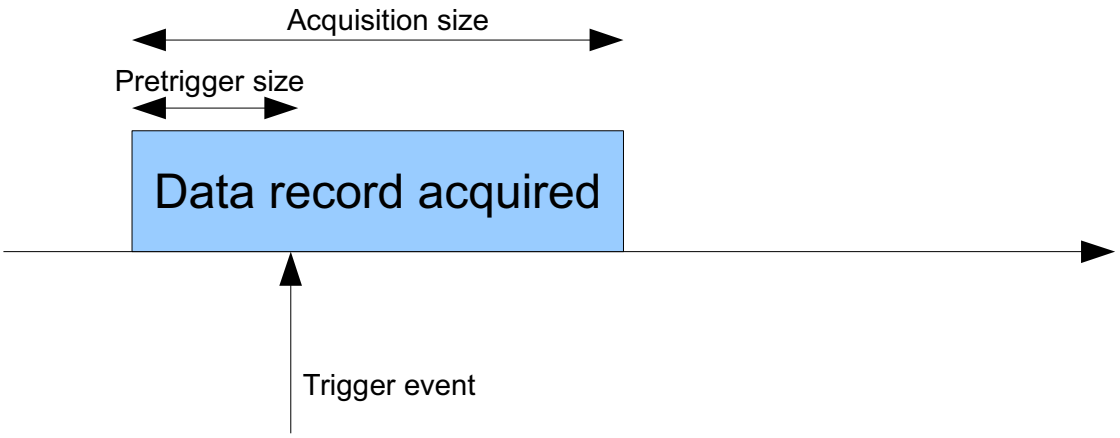


Figure 6: Pre-trigger buffer

3.2 Hold-off (Delay)

The trigger hold off is a delay from the trigger point to the actual acquisition starts, **Figure 7**. The size of the hold-off is up to 2^{34} samples (depends on digitizer model).

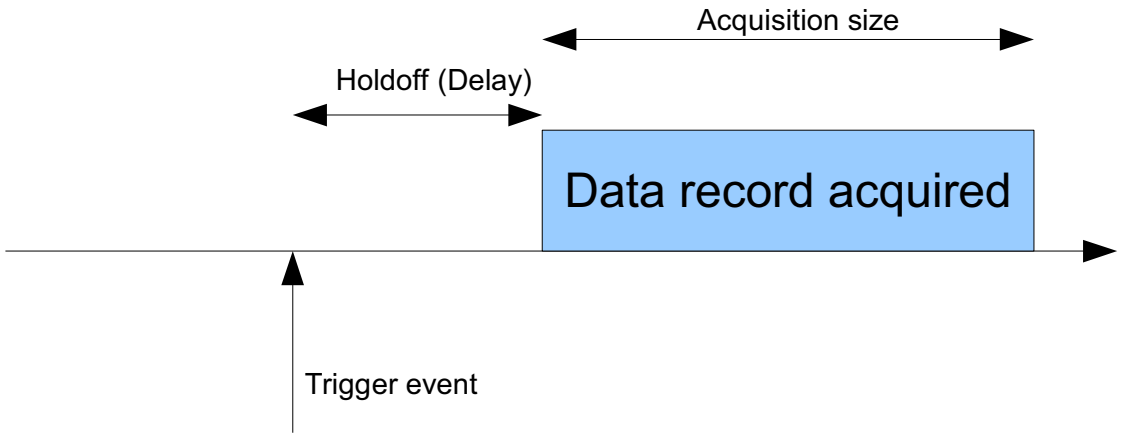


Figure 7: Trigger hold-off

3.3 Adjustable external trigger latency (ADQ V5)

When the data from the ADC is routed through signal processing in the custom user logic block, the latency may change. To compensate for that, the external trigger may be delayed a number of samples by built in delay line. See **Figure 8** for details. The effect is very similar to trigger hold-off, bu the intension is to make the trigger hold-off function neutral to custom logic. The command for adjusting the latency are

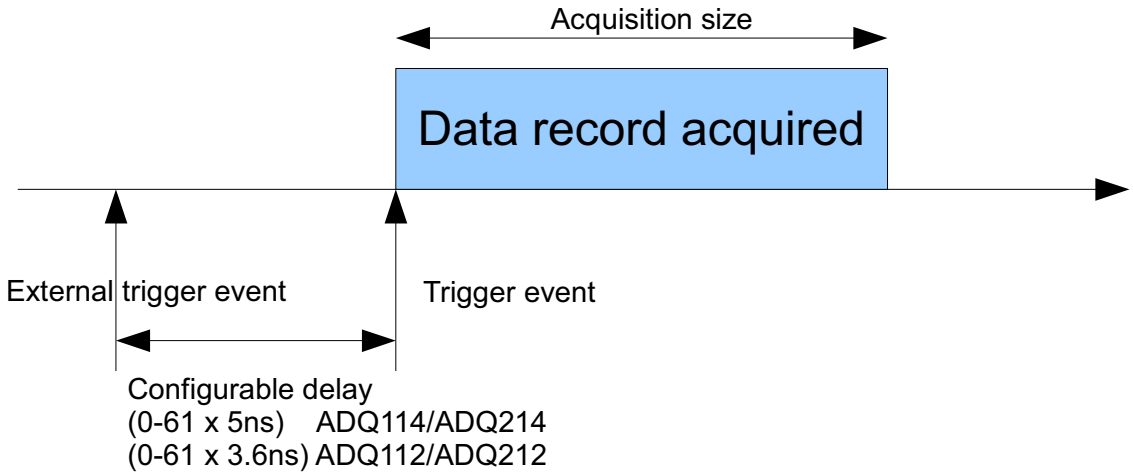


Figure 8: External trigger latency

4 Trigger output functions

The trigger port can be configured as an output, with different available output functions. The output functions are controlled by 2 multiplexers, one for data and one for output enable. Each

multiplexer selects among a set of available signals. By using the two multiplexers, the trigger output gets different functions:

The “data” multiplexer directly drives the output high or low. The output is driven high or low and may directly trigger other devices.

The “enable” multiplexer drive the output enable pin of the output buffer. The output is high-Z when enable is low. This means that the enable multiplexer may be used for wired-OR configuration between several digitizers. See **Section 7.2** for an example of usage.

ADQ V5 family specific: The output and input triggers are in the same physical connector. The default function of the external trigger is as an input port. The external trigger input is always active, even when the output is enabled. Thus and output signal may trigger the ADQ itself. This feature is used for synchronizing several ADQs.

ADQ V6 family specific: The output and input triggers are physically separated to two different connectors. The the direct path from trigger out to trigger in is instead available as an internal connection in the FPGA by selecting trigger mode 5, **Figure 4**.

4.1 Register set by application

Output level is controlled by the user’s software. Use the SetConfigurationTrig() or SetDirectionTrig() to activate output. Use the WriteTrig()-command to set the value of the trigger.

4.2 Output trigger state

Output is a copy of inversed waiting for trigger state in collect control block. This means that a rising edge will occur for each triggered record in synchronization with the data in the record. The falling edge will occur when the next record is ready to be triggered. If streaming, this rising edge will only occur once per streaming start.

The meaning of trigger state is depending on the data read out method. In streaming mode, trigger state is set while the streaming is ongoing. In batch mode, trigger state is set when the device is in a not waiting for trigger state.

4.3 Output level trigger events

Output is a copy of the level trigger event, regardless of whether this is allowed as trigger or not. Level trigger event is connected to output enable of the trigger output. This means that the output value is set by the register content. Use WriteTrig()-command to set the register to high.

4.4 Output trigger events

Output is a copy of the trigger event, only allowing correctly configured trigger events. A trigger here is not necessarily accepted by the Collect Control. Trigger event is connected to output enable of the trigger output. This means that the output value is set by the register content. Use WriteTrig()-command to set the register to high.

4.5 Output internal trigger

Output is a copy of the internal trigger event.

5 Trigger in ADQ Development kit

ADQ Development Kit enables integration of custom firmware for real time signal processing in the FPGA. The trigger unit supports custom integration. The signals marked with a Salmon

colored circle in **Figure 4** are available for the user in the ADQ Development Kit. These signal may be used for triggering custom function. The signals are of two types

- Where the line is terminated in a circle, it is possible to listen to the signal at that node.
- Where the circle circumference a wire, it is possible to break the wire and listen to the incoming value. It is also possible to inject a custom trigger at these nodes.

The ADQ Development Kit is purchased separately.

6 Support for synchronizing units

6.1 Trigger input blocker GPIO#5

The GPIO pin #5 may be used for blocking trigger. The communication interface does not allow for broadcasting arm trigger command. This means that trigger unit will be activated at a different time in different units. If, for example 2 units are connected to the same external trigger, they may start triggering at different times; when getting their arm trigger command. A way of doing that his to block triggers with GPIO#5. This is a logical signal that may be broad casted from one master unit to a number of slave units. in this way, units may start triggering simultaneously.

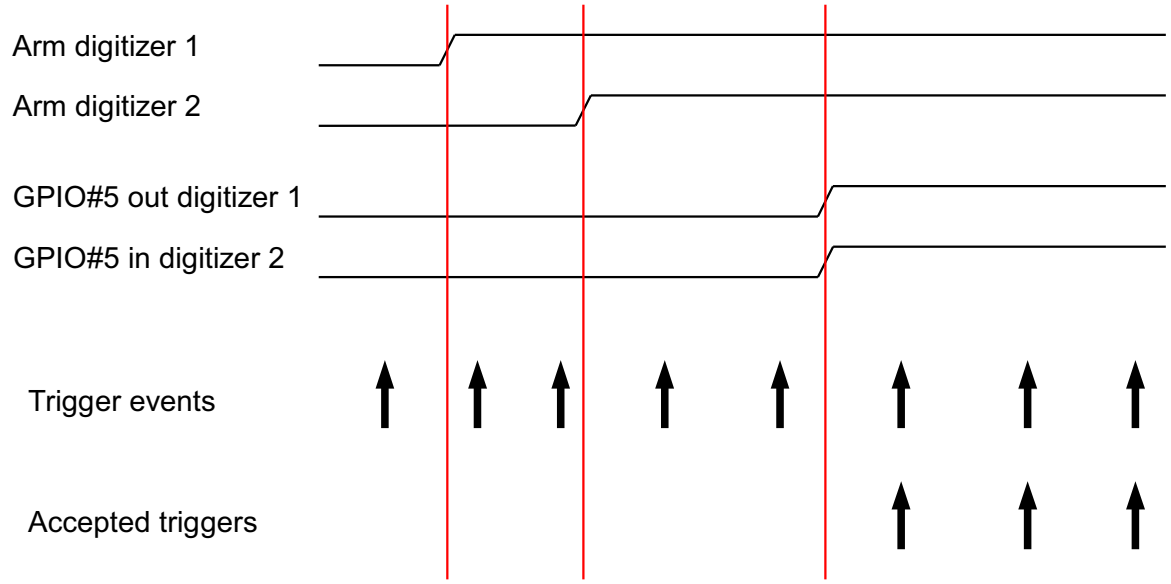


Figure 9: GPIO#5 Trigger block

6.2 Level trigger

The level trigger unit is always tracking activities and generating detection signals, even when another trigger input is selected. By feeding the level trigger to the trigger output, a broadcasting of a level trigger event is possible.

6.3 Broadcasting trigger on ADQ V5

For building a multi-channel system with several digitizers, it is useful if several digitizers can trigger each other. In this way, any channel in the system can trigger all digitizers. For this, a boolean OR function on the trigger is required. By using the output enable function in the trigger driver circuit, this OR function is implemented as a wired-OR.

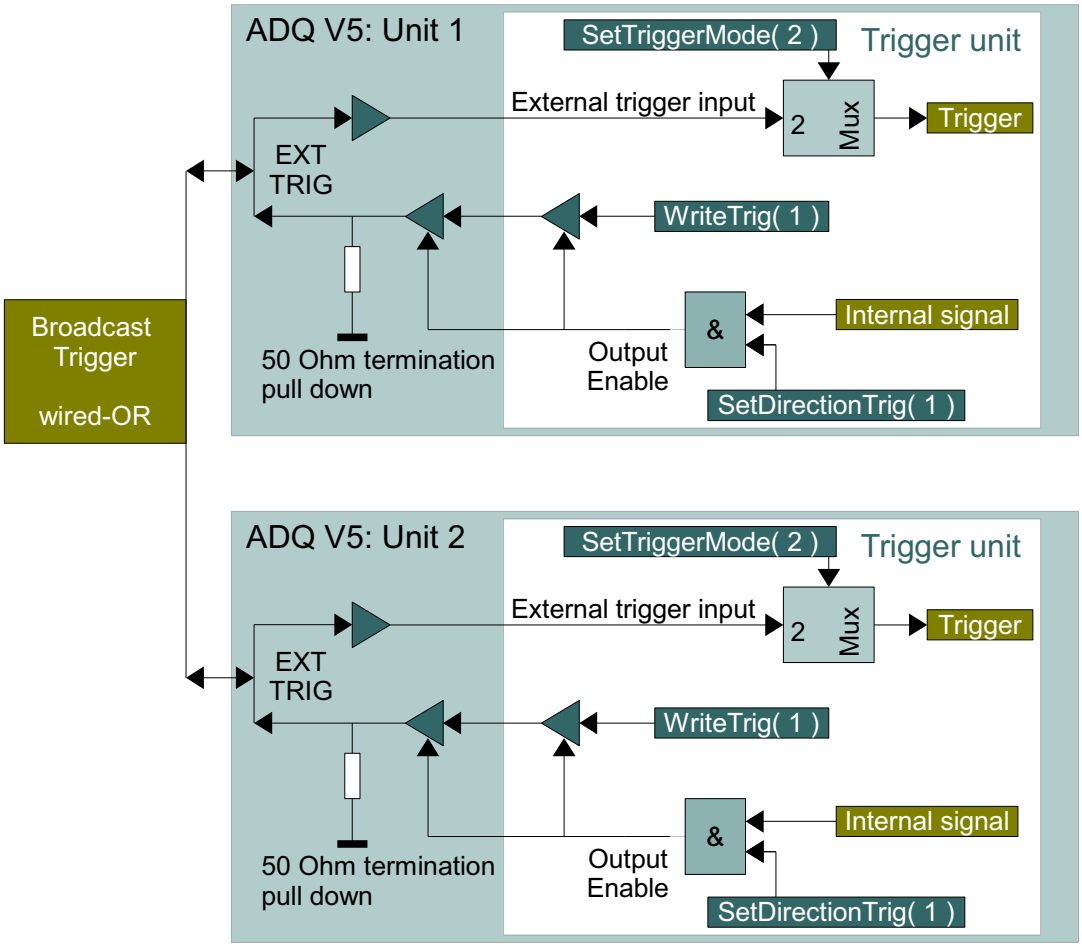


Figure 10: Broadcasting trigger by wired-OR.

6.4 Clock reference

The external clock reference is also a key component in trigger synchronization. For a fully synchronous system, the phase of the sampling clock has to be controlled. This is done by using a common clock reference for all units.

Note that this is not required is a slip of one sample is allowed between the units.

6.5 Differential Star triggers in PXI Express backplane

The PXI Express standard allows for precise trigger distribution via the backplane. ADQ V6 supports PXI Express star triggers.

7 Configuration examples

7.1 Triggering several digitizers in sync

The trigger out signal can be used to build a system where a set of digitizers are triggered synchronous, **Figure 11**.

The operation is then:

1. Select external trigger
2. Set trigger to input on slave units.
3. Set trigger output on master unit.
4. Arm the trigger in all units
5. Trigger all the units by setting trigger output to logic high in the master unit.
6. Up-load acquired data from all units.

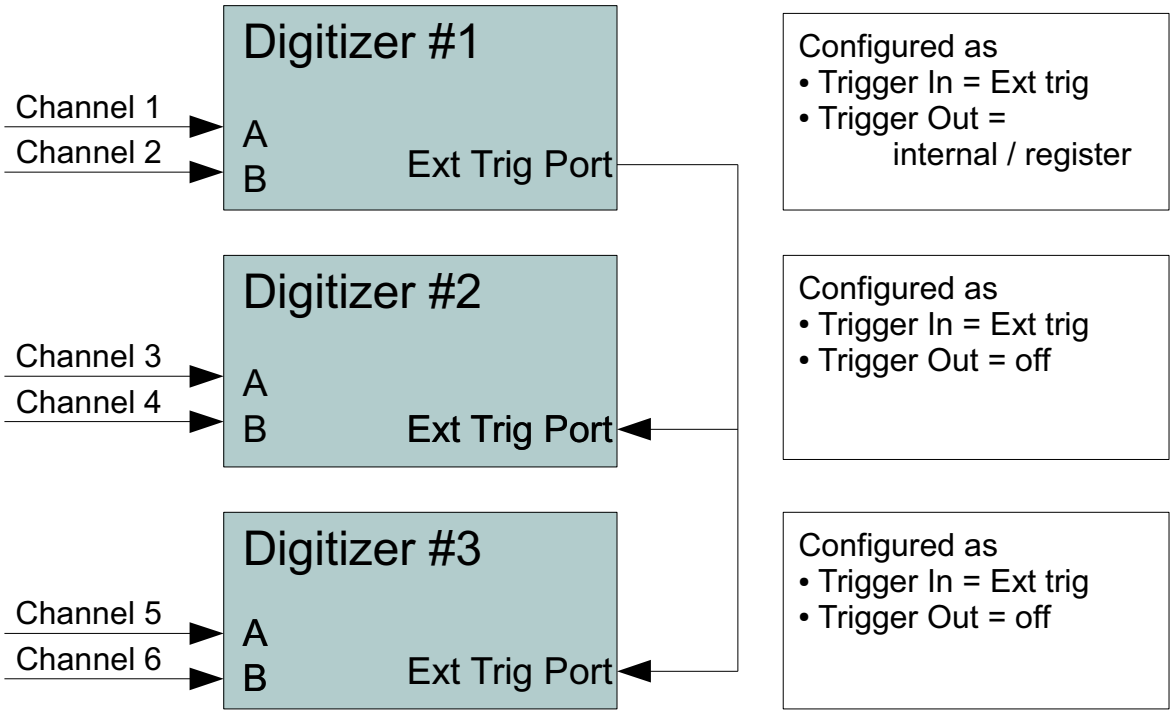


Figure 11: Trigger several units.

Use the trigger hold-off and pre-trigger settings to adjust for the latency.

7.2 Triggering 4 channels level trigger on ADQ214.

The ADQ214 has only 2 input channels. To design 4 (or more) channel system, the techniques in **Section 6** can be used in the system in **Figure 12**. The result is that a valid level trigger will generate a pulse on the trigger output port. This pulse will trigger data acquisition on all units.

1. Connect trigger signals with a cable between the units. (**Section 6.3**)

2. Connect GPIO with a cable between the units. (**Section 6.1**)
3. Set level trigger parameters in all units.
4. Select external trigger as trigger source in all units.
5. Set GPIO#5 as output in master.
6. Set GPIO#5 as input in slave.
7. Activate GPIO#5 trigger blocker in all units (CFGMODE = 0x39)
8. Set level trigger to control output enable (CFGMODE = 0x39) (**Section 6.2**)
9. Set Register trigger as trigger out (CFGMODE = 0x39)
10. Write “1” to Register.
11. Arm trigger in all units.
12. Write a “1” o GPIO#5 in master unit.

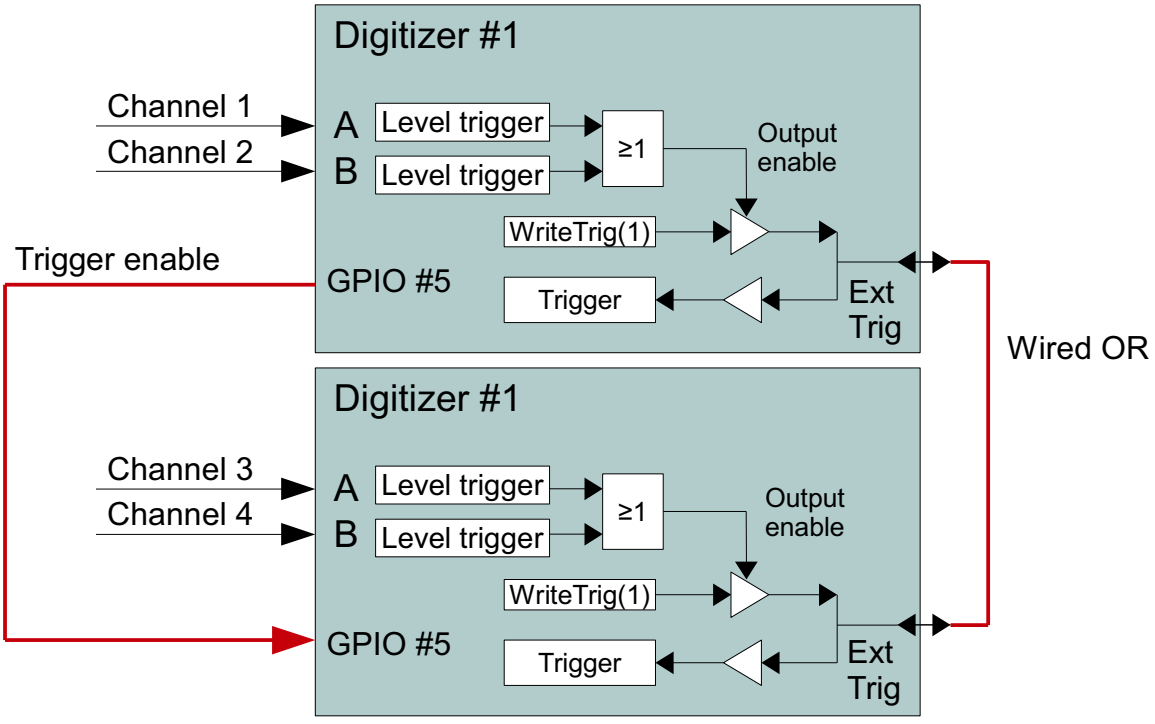


Figure 12: 4 channels level trigger

Note 1: The time for the trigger signal to get to the from the master to the slave depends on the cable length and quality. Even for a high quality short cable it is in the order of the sample period. This delay is in the same order as the delay from the various analog sources in the experiment and has to be taken into a account in a potential calibration procedure.

Note 2: The phase of the ADC clocks may differ on the boards. This is handled by the enhanced trigger accuracy feature, which determines the trigger position relative the clock phase on 1/4 of the sample period. (**Section 8**)

Note 3: Use external clock reference to lock the clocks in the digitizers. (**Section 6.4**)

7.3 Using the internal trigger for other equipment triggering

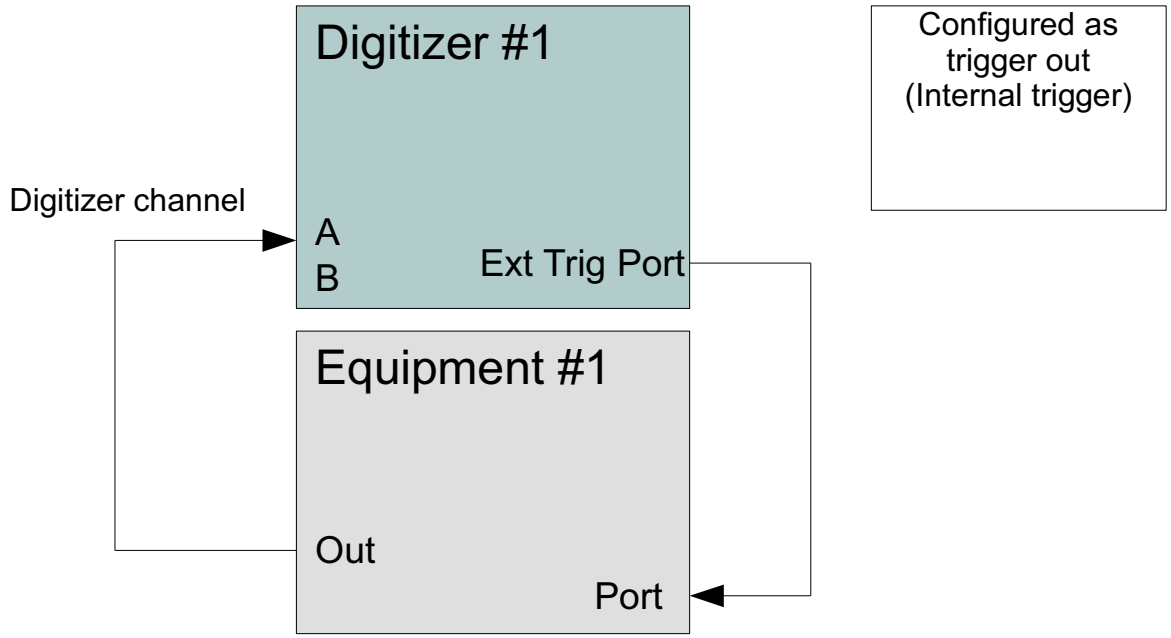


Figure 13: Trigger external equipment

Use the powerful internal trigger to trigger external equipment.

Connect the trigger output to the trigger input of an external equipment.

It is possible to trigger the digitizer by the same trigger as the external equipment. Then select external trigger on ADQ V5 or internal trigger on ADQ V6. Use Trigger hold-off and pre-trigger settings in the digitizer to adjust the timing between the units.

The internal trigger may also be used to trigger the external equipment only and the digitizer may be level triggered. Then there is a completely event driven measurement loop.

7.4 External clock and trigger in a synchronous system

If an external trigger unit is available (or required), use the system set-up is in **Figure 14**. The trigger unit is preferably synchronized (phase locked) with the clock for best result, but that is not strictly required. The external clock (or the external clock reference) is used to achieve accurate synchronous sampling in all units.This is specially important for long records[1]. If the data records are short, the internal clock may be good enough.

1. As an example: if the clock accuracy is 1 ppm and the data record is 10 M samples, there might be 10 samples mis-alignment in the end of the records in different digitizers. This is solved by an external clock reference. Note that this is not a problem between channels within the same unit, since they operate on the same clock.

The digitizers are addressed one by one. It is not possible to broadcast commands. If the trigger source can be fully controlled, stop the trigger when arming the units. If the trigger signal is running continuously, use th GPIO#5 to block the trigger.

1. Set up external clock reference or external clock source.
2. Set up external trigger.
3. Set the GPIO pin 5 in Digitizer #1 to out logical low.
4. Set the GPIO pin 5 in Digitizer #2 to input.
5. Set up the trigger to include the GPIO#5 blocker.
6. Arm the triggers in all units.
7. Write a logical high to the GPIO#5 in Digitizer #1. The triggers in the units are released.
8. The next trigger event triggers all devices.

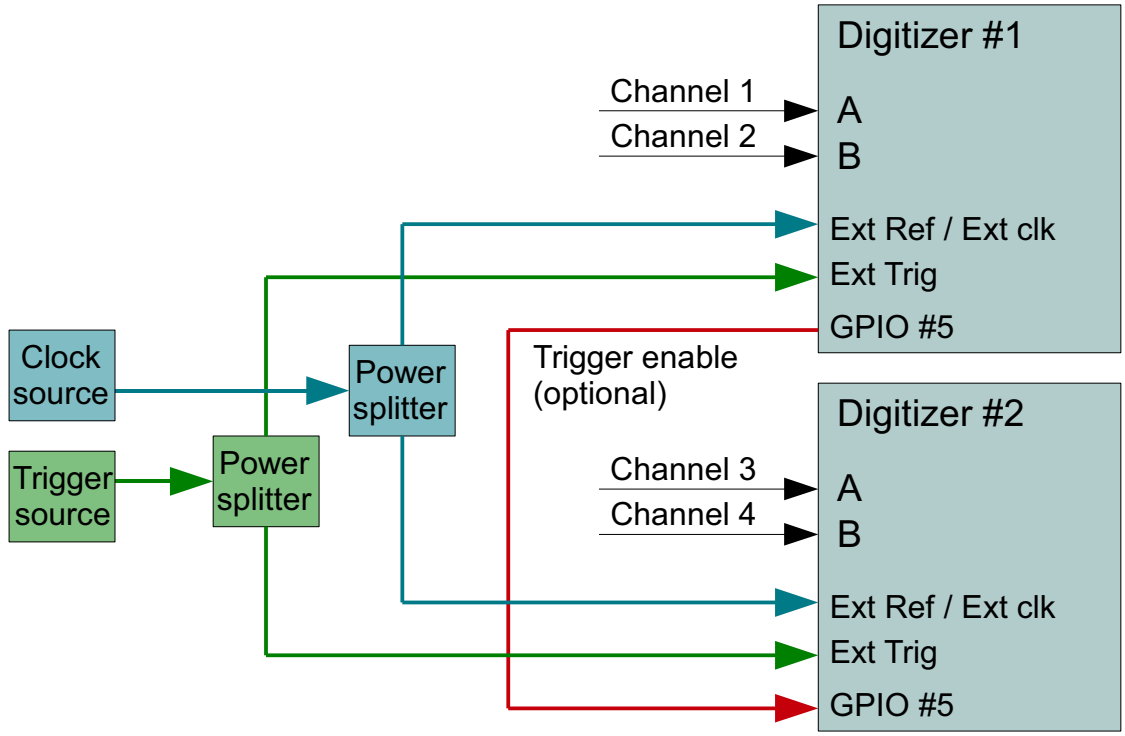


Figure 14: Measurement set-up. External trigger source.

7.5 Example code

The MATLAB examples code ADQ214_4_ch_level_trig.m and ADQ214_4_ch_external_trig.m illustrate how to use the synchronization. The output from an evaluation setup is in **Figure 14**. The channel B and D are connected to the same source in order to verify the simultaneous triggering of the two Trigger . MATLAB code ADQ214_4_ch_level_trig.m and ADQ214_4_ch_external_trig.m are available on the product CD.

8 Enhanced trigger accuracy

8.1 Enhanced trigger accuracy in ADQ214

In a standard set-up, the time stamp of a data is set only by the sampling clock. The time resolution is then only $1/f_S$, that is 2.5 ns for f_S = 400 MSPS. The trigger in ADQ214 is however sampled by 4 X f_S.The trigger resolution is thus 625 ps. This enhanced trigger accuracy can be used to align data vectors from a set of measurements where the trigger is not phase locked to the sampling clock.

The enhanced timing information is accessed from the multi-record header, **Section 9**. In header word number 2 bit 16 and 17, the offset between the trigger event and the sampling clock, **Table 4**.

BIT 17	BIT 16	TRIGGER OFFSET IN SAMPLE PERIODS
0	0	0
0	1	1/4
1	0	2/4
1	1	3/4

Table 4: Trigger offset code

The alignment of data can be done by adjusting the time scale for each vector, **(1)**.

adjusted time = original time + trigger offset. (1)

Trigger offset is from **Table 4**. The units in **(1)** is sample index.

Another method is to interpolate data to corrected sampling times, **(2)**.

adjusted data (n) = data (n+1) - trigger offset (data (n+1) - data (n)) (2)

The interpolation is illustrated in **Figure 18**.

8.2 Example code

The MATLAB example code **ADQ214_accurate_trigger.m** illustrates how to use the enhanced trigger accuracy. The example contains code for read out of the trigger offset information. The wave forms are adjusted according to **(1)** and **(2)**. The example also contains a trigger analysis, see **Section 8.3**.

8.3 Trigger analysis set up

A **typical** measurement set-up is shown in **Figure 15**. Signal source is a square wave generator. High precision instrument is not required. 10 kHz is only an example of frequency setting. The amplitude has to be large enough to trig the Trigger even after the power splitter. The signal generator must **not** be locked to the sampling clock. The evaluation rely on the pseudo time noise generated by two drifting oscillators. The filter on the signal to channel B generates a ramp of the trigger edge. The ramp is locked in time to the trigger event. The timing of the ramp can be accurately determined and thus the time of the trigger event can be analyzed.

The result of the analysis shows that the trigger uncertainty is reduced by a factor of 4. The original data in **Figure 16** spreads across an entire sampling period in time. The accurate trigger information is used for adjusting the time scale **(1)**, which gathers the curves to within 1/4 of a sampling period, **Figure 17**. The interpolation in **(2)** yield the same result, **Figure 19**.

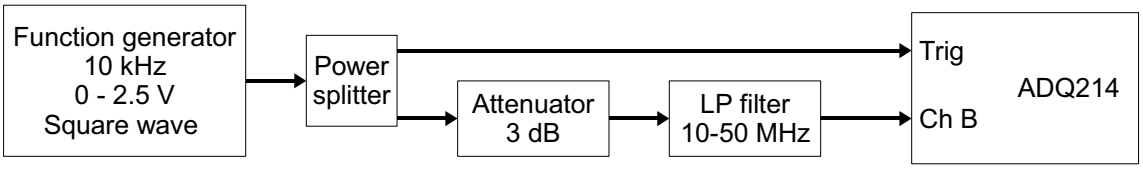
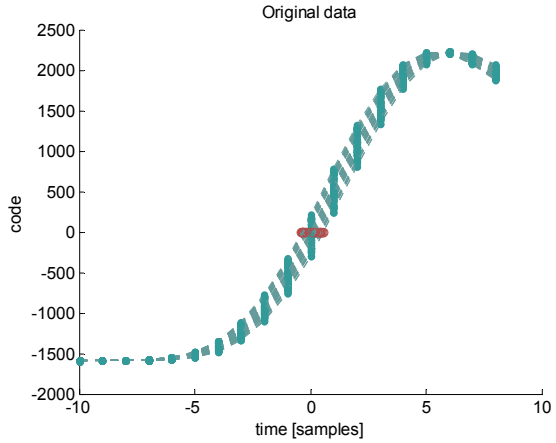
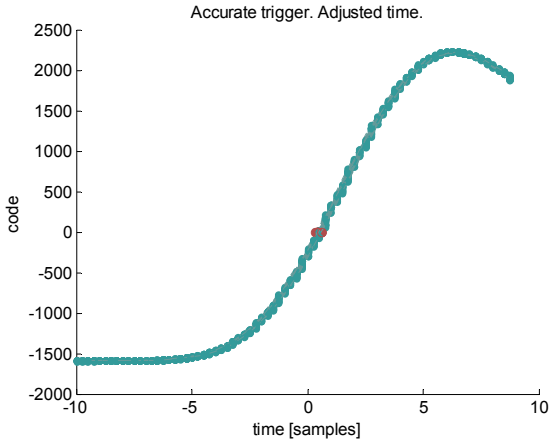


Figure 15: Measurement set-up. Example is for channel B. Channel A is equivalent.



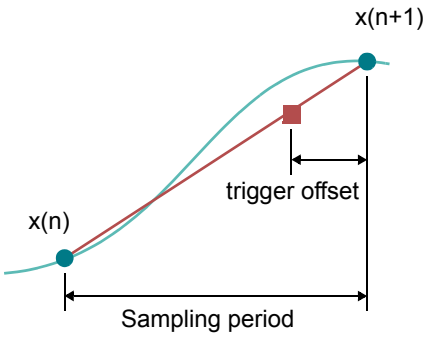
Spread	+/- 0.5 samples
Standard deviation	0.28

Figure 16: Original data



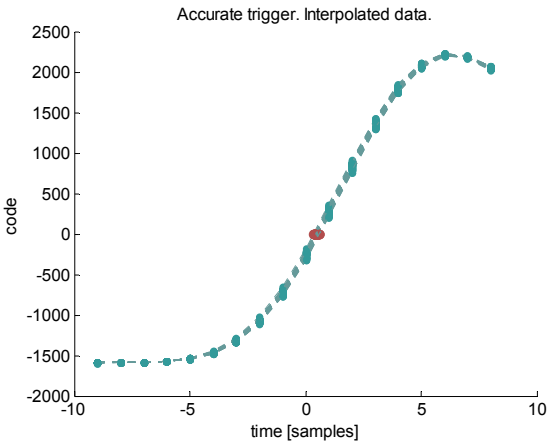
Spread	+/- 0.125 samples
Standard deviation	0.069

Figure 17: Adjusted time vector



trigger offset	Accurate trigger data
x	Data vector
n	Time index

Figure 18: Interpolation principle



Deviation	+/- 0.125 samples
Standard deviation	0.066

Figure 19: Interpolated data.

8.4 Reference

MATLAB code ADQ214_accurate_trigger.m is available on the software CD.

9 Trigger information in record header

9.1 Multi record header

All trigger information is available in the multi record header. The multi record mode uses the DRAM as data buffer. In the DRAM, data is formatted to fit the hardware physical constraints. Most of the information is thus only used by the API to unpack the record and is not of value for application usage.

However some field are intended for applications. The parameters are described in **Table 5**. The location in the headers are in **Table 6** and **Table 7**.

There are several API functions for retrieving this information. GetMultiRecordHeader() will return all this information.

PARAMETER	DESCRIPTION	FAMILY
Extended trigger	Extended trigger accuracy	V5
Total triggers	Number of accepted triggers since the digitizers was started or reset.	V5 V6
Acquisition triggers	Number of accepted triggers since arm. This is expected to be the same as record number.	V5 V6
Time stamp	Real time counter	V5 V6

Table 5: Parameters in record header

WORD 0																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				Trigger word within a memory page[1]																											

WORD 1																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				Memory page where trigger occurred[1]																											

WORD 2															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved												Extended trigger			
15	14	13	12	11	10	9	8	7	6	5	4				
Reserved												Trigger within word[1]			

WORD 3																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Total triggers (since start)																													

WORD 4																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Acquisition triggers (since arm command)																													

WORD 5															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved												Trigger type			

WORD 6																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Time stamp. Bit [31:0]																													

WORD 7																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Time stamp. Bit [63:32]																													

Table 6: Multirecord header ADQ V5.

1. Used by API only.

WORD 0																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				Trigger word within a memory page[1]																									

WORD 1																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved				Memory page where trigger occurred[1]																									

WORD 2															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved													Trigger type		
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
External trigger vector[1]															

WORD 3																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Total triggers (since start)																													

WORD 4																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Acquisition triggers (since arm command)																													

WORD 5																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Level trig vector[1]																													

WORD 6																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Time stamp. Bit [31:0]																													

WORD 7																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Time stamp. Bit [63:32]																													

Table 7: Multirecord header ADQ V6.

1. Used by API only.

9.2 Streaming record header

The streaming record header contains trigger information. In the streaming mode, data is already correctly aligned to the trigger when fetched by the API. The header information is thus only for the application to use. The parameters are described in **Table 8**. The location in the header is in **Table 9**. Streaming header is 16 bytes.

PARAMETER	DESCRIPTION	FAMILY
Record counter	Number on this record since start. This value will wrap at 2^{32}. Individual values for each channel in the device.	V5 V6
Serial Number	Register value. Intended for serial number of the digitizer in integer format. Note that the API sets this value, but the user may change it by a command[1].	V5 V6
Register value	Arbitrary register value to be set by the user[2].	V5 V6
Ext Acc	Extended trigger accuracy. This is used in some models and some trigger modes only. In other models and for other trigger modes, the field is reserved for future use.	V5
Channel	Channel number.	V5 V6
Time stamp	Real time counter	V5 V6

Table 8: Parameters in streaming record header

1. Availability TBC
2. Availability TBC

WORD 0																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Record counter																															

WORD 1																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Serial number																Register value								Ext. acc.				Channel			

WORD 2																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Time stamp. Bit [31:0]																															

WORD 3																													
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Time stamp. Bit [63:32]																															

Table 9: Streaming record header ADQ V5 V6. TBC

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